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High-Performance Audio Power Amplifier with a Push-Pull Voltage Amplification Stage and Active Loads in the Input Differential Pair

Amplificador de Áudio de Alto Desempenho com Cargas Ativas no Par Diferencial de Entrada e Estágio de Ganho de Tensão Push-Pull

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ABSTRACT

The paper proposes an innovative way to connect a differential stage with a current mirror as its load to a voltage amplification stage (VAS) without using gain-limiting resistors, employing a “buffer-bias” stage to stabilize the VAS current and preserve circuit performance. The effectiveness of the proposed topology was demonstrated through measurements on a functional prototype, which exhibited high amplifier performance, such as a total harmonic distortion of 0.0008% at $1\,\text{kHz}$ even at full power ($50\,\text{W}_{\text{RMS}}$) and a slew rate of $107.4\,\text{V}/\mu\text{s}$.

keywords power amplifier, symmetrical, complementary, push-pull, active loads

RESUMO

O artigo propõe uma forma inovadora de se conectar um estágio diferencial com espelho de corrente como carga a um estágio de amplificação de tensão (VAS) sem o uso de resistores limitadores de ganho, empregando um estágio “*buffer-bias*” para estabilizar a corrente do VAS e preservar o desempenho do circuito. A eficácia da topologia proposta foi demonstrada por meio de medições realizadas em um protótipo funcional que demonstraram o alto desempenho do amplificador, tais como: distorção harmônica total na ordem de $0{,}0008\%$ a $1\,\text{kHz}$ mesmo à potência total ($50\,\text{W}_{\text{RMS}}$) e *slew rate* de $107{,}4\,\text{V}/\mu\text{s}$.

palavras-chave amplificador de potência, simétrico, complementar, *push-pull*, cargas ativas

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Introduction

High-performance audio amplifier manufacturers make great efforts to optimize circuits and improve their performance in every possible way. However, when it comes to symmetrical topologies, they often leave one of the most fundamental building blocks untouched: the resistive load of the differential pair, known as the Long-Tailed Pair (LTP), which should be replaced by a current mirror (CM) for maximum performance.

The use of a CM offers clear benefits, including its ability, in conjunction with the LTP, to actively supply and absorb current from the Voltage Amplification Stage (VAS). This results in equal slew rates (SR) for both rising and falling edges, reduced generation of odd harmonics in the input stage due to improved current balancing in the differential pair, and effectively doubles the transconductance of the LTP (Cordell, 2019; Slone, 1999).

However, the symmetrical topology with a CM presents challenges, such as the undefined voltage at the collector of the left transistor in the current mirror, which impacts the stability of the voltage at the base of the VAS. A common solution, employed by Cordell and REVOX in their B242 amplifier model, involves using resistors in the LTP to differentially load the input pair. This approach allows the VAS to operate with a defined current but at the cost of reduced open-loop gain (OLG).

This work proposes a different approach, where the differential pair is kept free of any additional resistive load. Instead, the quiescent current of the VAS is defined by a separate stage, called the buffer-bias stage, which preserves the performance of the LTP and stabilizes the VAS current without reducing the OLG.

This article is organized as follows: the Materials and methods section provides a brief description of the conventional topology of audio amplifiers, followed by an explanation of the problem studied and the proposed solution. In the Results and discussion section, we present the performance data obtained from measurements of the developed prototype, highlighting the effectiveness of the proposed topology. The final section outlines the conclusions of this study.

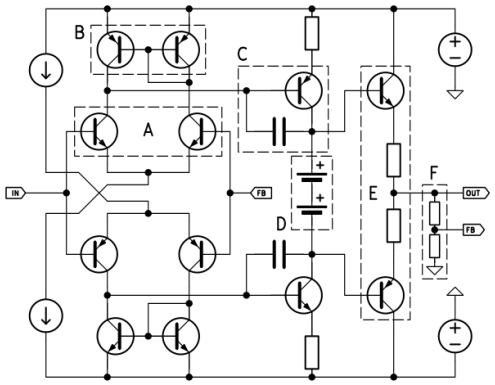
Materials and methods

This section presents the basic topology of audio amplifiers and introduces the problem addressed in this study. After that, we describe the proposed solution and the methodology adopted. To demonstrate the effectiveness of the suggested topology, a complete audio amplifier design is developed, resulting in a prototype intended to validate the expected outcomes. The design was conceived to achieve a satisfactory balance among performance parameters; however, focused optimization can be performed to prioritize specific parameters, as suggested by Visintin et al. (2022).

The problem addressed

Figure 1 illustrates the basic components of a standard audio amplifier, described here for a clear understanding of the problem addressed: input differential pair (A), current mirror (CM) (B), voltage amplification stage (VAS) (C), VBE multiplier (D), output stage (E), and feedback network (F).

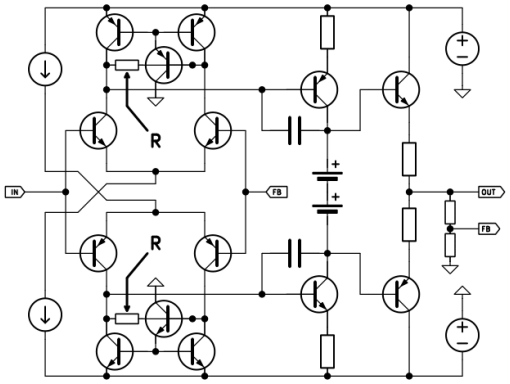
Figure 1 - Symmetrical VAS with undefined current.



The topology shown in Figure 1 is considered impractical without the application of additional techniques, as there is a problem where the left transistor of the CM fails to develop a well-defined collector voltage. Consequently, the voltage at the base of the VAS is also undefined, and there is no predictable voltage across its emitter resistor, which determines the VAS current.

As shown in Figure 2, Cordell (2019) used a method quite similar to the one employed by the Swiss manufacturer REVOX in their B242 model released in 1986 (Revox B 242, 2019). In this method, resistors (marked with "R" and arrows) through the LTP apply a differential loading to the input pair.

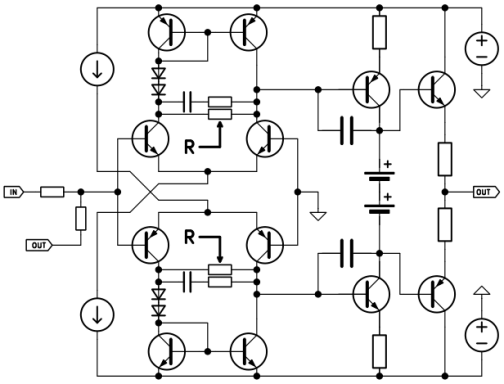
Figure 2 - Method used by Bob Cordell.



Adapted from *Designing Audio Power Amplifiers*, by Cordell, B. Routledge, 2019.

A simplified version of the circuit used in the commercial B242 amplifier is illustrated in Figure 3.

Figure 3 - Simplified circuit of the REVOX B242.



Adapted from Revox B242, 2019.

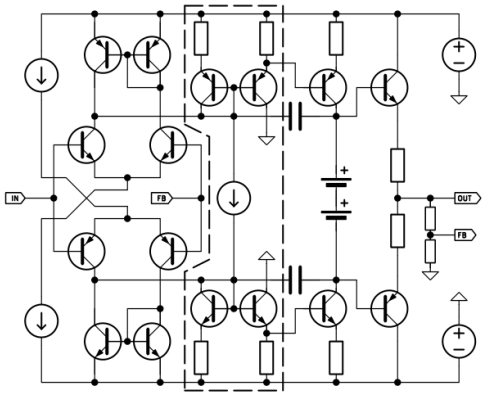
The resistor, shown in Figure 2, transfers both the AC signal and the DC bias to the opposite branch of the LTP, which is directly connected to the VAS. As a result, the amplifier now operates at the cost of a reduced OLG due to the resistive loading imposed on the LTP and the current flowing through the VAS is no longer indefinite.

The method adopted in this study keeps the differential pair free from any additional loading imposed by resistive elements, as seen in Figures 2 and 3. Instead, the quiescent current of the VAS is defined by a separate stage. This additional stage, highlighted with dashed lines in Figure 4, will be referred to as the buffer-bias stage.

Proposed circuit

This section is dedicated to the description of the purpose and operation of each of the ‘blocks’ that compose the proposed circuit. Each block will be detailed in the following order: input filters, input differential pair, buffer-bias stage, voltage amplification stage, VBE multiplier, output stage, output filters, and DC offset servo.

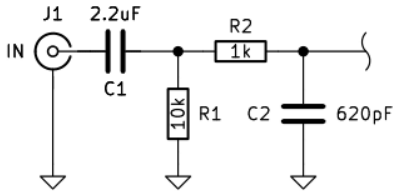
Figure 4 - Simplification of the proposed topology.



Input filters

The low-pass and high-pass filters are shown in Figure 5. The function of these filters is to attenuate spurious signals that do not contain audio information without interfering with the amplifier's transient response. The calculated values result in lower and upper cutoff frequencies of $f_{CL} = 7.2\,\text{Hz}$ and $f_{CH} = 256.7\,\text{kHz}$, respectively. C1 is a polyester film capacitor, while C2 has a Class I dielectric (C0G/NP0). These types are suitable for use in these positions as they introduce minimal distortion (Kaye, 2020).

Figure 5 - Band-pass filter at the amplifier input.

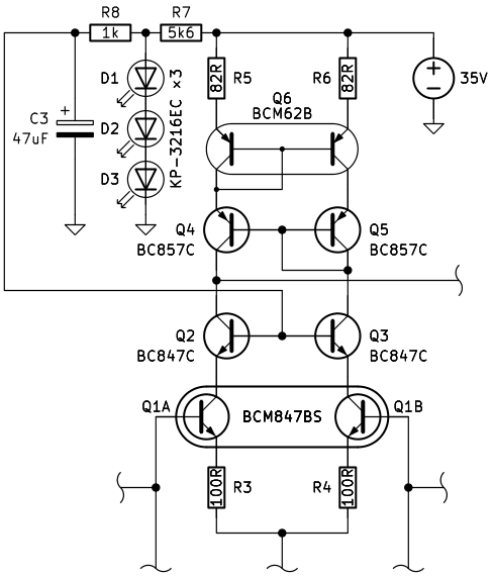


Input differential pair

For the transistors in the differential pair, the BCM847BS and its complementary PNP counterpart BCM857BS were chosen, as they are matched pairs ideally suited for this type of application. However, they come in the tiny SOT-363 package, with a thermal resistance of 416°C/W from junction to ambient.

To limit power dissipation in the transistors, a cascode configuration was used, formed by Q2 and Q3, as illustrated in Figure 6. This configuration provides the benefits of limiting the differential pair's power dissipation while also enhancing immunity to Miller and Early effects (Abidi, 1988).

Figure 6 - Input differential pair (upper section).



The voltage reference for cascode biasing comes from a branch of three red LEDs connected in series (Kingbright KP-3216EC). This combination (D1 to D3) generates approximately $V_{CAS} = 5.4\,\mathrm{V}$ under a 5mA current.

The current flowing through the LTP is 6mA, meaning the power dissipation in each transistor within Q1 is calculated as shown in equation (1):

$$P_D = I_C \times \left(V_{CAS} - V_{BE_{Q2/Q3}} + V_{BE_{Q1}}\right) = 16.2[\,\mathrm{mW}], \tag{1}$$

where I_C is the collector current for each branch of the LTP (3 mA), and $V_{BE_{Q1}}$ and $V_{BE_{Q2/Q3}}$ cancel each other out, resulting in a dissipation of approximately 16 mW. This, in turn, increases the package temperature by 13 °C above ambient temperature.

Above the cascode, as shown in Figure 6, there is an active load composed of transistors Q4 to Q6, forming a Full Wilson Current Mirror. This topology offers more advantages than a classic two-transistor current mirror (Wilson, 1981).

In a simpler current mirror, one transistor is configured as a diode, while the other operates in the active region. This can lead to a significant difference in power dissipation levels between the transistors since the collector-emitter voltage (V_{CE}) of the active transistor can be dozens of volts, while the V_{CE} of the BJT-diode is only its V_{BE}.

This high voltage on the active transistor also causes an undesirable base-width modulation effect, which reduces the output resistance of the BJT, making the current mirror even less ideal. The full Wilson current mirror solves this issue by adding transistors Q4 and Q5, which equalize the collector voltages of the two Q6 BJTs.

Special components were selected for the BJTs in the current mirrors: the BCM62B (dual PNP) and the BCM61B (dual NPN). These are also matched pairs of BJTs within a SOT-143 package, with their bases internally connected, as in a classic current mirror (CM).

Regarding the emitter resistors of the CM, a value of 82 Ω was chosen to avoid a significant voltage drop while providing a resistance ratio of approximately 10:1 with the intrinsic emitter resistance (r'_e) of the BJTs, as given by equation (2):

$$r'_e = \frac{25.8\,\mathrm{mV}}{I_C\,[\mathrm{mA}]} = 8.6[\,\Omega]. \tag{2}$$

The use of emitter degeneration in current mirrors provides benefits such as improved noise performance, increased output resistance, and better matching between the BJTs (Bilotti & Mariani, 1975).

In the case of the emitter resistors of the LTP, a value of 100 Ω was chosen, which is approximately 12 times the intrinsic emitter resistance of each transistor in the LTP. Emitter degeneration in common emitter gain stages linearizes the stage and increases its bandwidth, although at the cost of a reduction in transconductance (Sedra & Smith, 2019).

Figure 7 illustrates the current source (CCS), responsible for defining the current through the LTP. This current is set in the right branch and mirrored to both LTPs. The mirrors are again emitter-degenerated, this time by 43 Ω in a 10:1 ratio with r'_e, and resistors R11 to R13 are present to reduce voltage and dissipation across other parts of the circuit.

Figure 8 details the CCS blocks, where currents are defined by adjustable integrated current sources (LM334), cascoded with JFETs to provide an even higher output impedance. The JFET in question is the MMBF4391, with V_{GS} measurements at 6 mA and 1 mA of $-5.83\,\mathrm{V}$ and $-5.65\,\mathrm{V}$, respectively. These values are far enough from the LM334's minimum operating voltage of 1 V, but not high enough to cause significant dissipation. The 6 mA source biases the LTP, and the 1 mA source biases the buffer-bias stage.

This block also includes a silicon diode used as a thermal compensation element to provide a temperature coefficient (tempco) close to zero. The diode chosen was BAV21W, with a measured tempco of around $-1.57\,\mathrm{mV/°C}$. Resistors R19 and R20 were selected based on the LM334 datasheet guidelines for the design of a zero tempco current source (Texas Instruments, 2000).

Figure 7 - Current mirror and current source (bottom part).

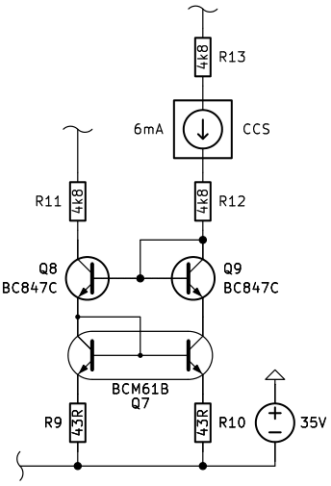
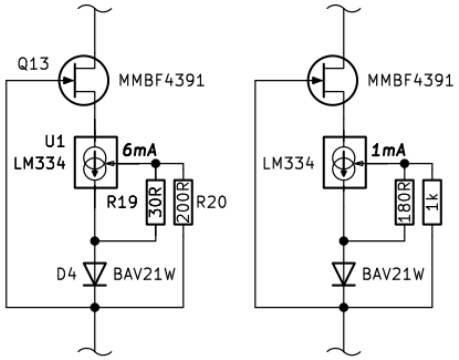


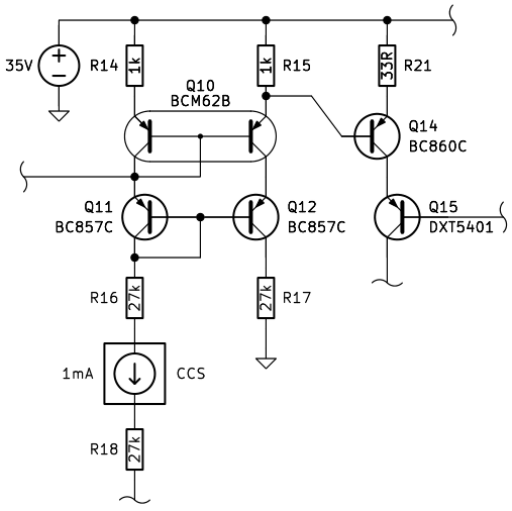
Figure 8 - Detailed view of the CCS block.



Buffer-bias stage

The buffer-bias stage is a distinctive feature of the topology addressed in this work and is responsible for its operation. It defines the current for the VAS while simultaneously isolating the signal through what can be seen as both a current mirror and an emitter follower. As shown in Figure 9, it consists of a cascoded CM with relatively high emitter degeneration. The cascoded CM is known for its very high impedance and good high frequency response due to reduced Miller capacitance (Harrison, 2005).

Figure 9 - Buffer-bias stage (upper part).



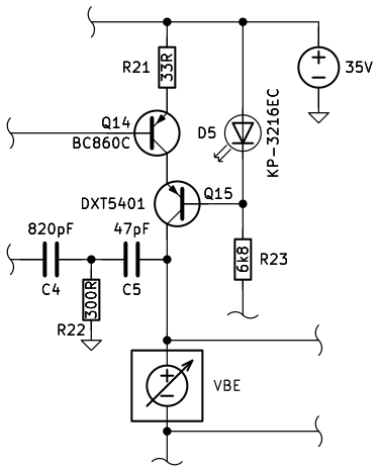
The current through this stage is defined by another CCS block containing an LM334, which generates a voltage across R15 since transistors Q10 to Q12 form a cascode current mirror, this voltage then gets the V_{BE} of the VAS transistor subtracted from itself and the remainder appears across the VAS emitter resistor (R21), thus setting the VAS's quiescent current.

The AC signal from the LTP is injected into the bases of transistor Q10, which is the active transistor in the CM but also conveniently functions as an emitter follower, and then the signal is passed on to the VAS. Resistors R16 through R18 are used to reduce power dissipation in the active devices to a level compatible with the SMD packages used.

Voltage amplification stage (VAS)

The upper branch forming the VAS is shown in Figure 10. This branch is subjected to approximately 10 mA of current and voltage variations that can extend up to the opposite rail. This results in power dissipation levels that require the use of medium-power transistors, but this additional robustness comes at the cost of reduced current gain (h_{FE}), a lower transition frequency (f_T), and higher parasitic capacitance (C_{OB}).

Figure 10 - Voltage amplification stage (upper part).



Another cascode is used in this stage, allowing the use of low-power transistors to be used in areas that would otherwise require medium-power devices, with the previously mentioned disadvantages. For the BJTs in the VAS, the BC860C and its complementary NPN (BC850C) were selected due to their good availability, high gain, low parasitic capacitances, acceptable noise performance, high transition frequency, and good gain linearity.

The transistors in the cascode are the DXT5401 and its complementary NPN (DXT5551). They were selected for their maximum V_{CE} rating of 150 V, relatively low collector capacitance of 6 pF, transition frequency above 100 MHz, and availability in the SOT-89 package, which supports the required power dissipation, when given a sufficient board copper area.

The reference voltage for the cascode is generated by D5, another KP-3216EC LED, biased at 5 mA. Its measured voltage was $V_{D5} = 1.82\,\mathrm{V}$. Subtracting $V_{BE_{Q15}} = 0.657\,\mathrm{V}$ and $V_{R21} = 0.343\,\mathrm{V}$ from V_{D5} gives a value of 0.82 V for $V_{CE_{Q14}}$, as determined by equation (3):

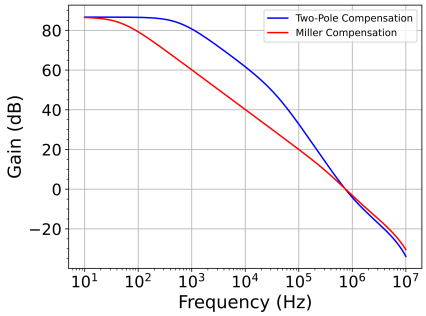
$$V_{CE_{Q14}} = V_{D5} - V_{BE_{Q15}} - V_{R21} = 0.82[\,\mathrm{V}]. \tag{3}$$

Since all amplifier sections are powered by the same $\pm 35\,\mathrm{V}$ rails, this low cascode voltage keeps the collector of Q14 as close to the rail as possible, ensuring that it does not limit the maximum voltage swing available to this stage and, consequently, the maximum output power.

For the compensation scheme, two-pole compensation (TPC) was chosen instead of the traditional Miller compensation (MC) because it offers the benefit of maintaining a higher gain over a wider frequency range (Roberge, 1975). Unlike MC, where the gain increases by 20 dB/decade as the frequency decreases below the crossover frequency point, TPC increases the gain by 40 dB/decade.

A comparison between the frequency responses of the amplifier using TPC and MC compensation types was generated using LTspice® software (Analog Devices, 2025) and is shown in Figure 11. A higher OLG means more gain is available for negative feedback to reduce distortions.

Figure 11 - Bode diagram – TPC versus MC.



The Bode diagram demonstrates that by implementing the compensation network shown in Figure 10, most of the gain increase occurs within the audible frequency range, which is desirable for higher fidelity in audio reproduction.

The TPC curve in Figure 11 uses the compensation network shown in Figure 10, while the MC curve was simulated by disconnecting R22. The capacitance of the series arrangement between C4 and C5 is approximately 44.5 pF.

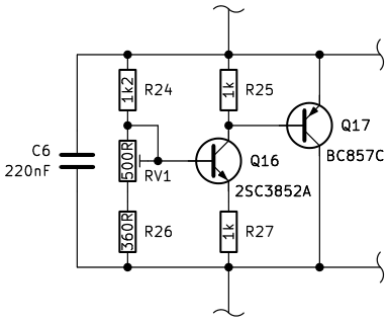
The maximum increase in gain at low frequency is achieved by introducing a zero near the crossover frequency. However, care must be taken as the phase margin decreases the closer the zero is positioned to the crossover frequency. The location of the zero is calculated by equation (4) (Dymond & Mellor, 2010)

$$f_Z = \frac{1}{2\pi R_{22}(\mathrm{C4} + \mathrm{C5})} = 611.9\,\mathrm{kHz}. \tag{4}$$

VBE Multiplier

Figure 12 illustrates the VBE multiplier (VBEM) block, which stabilizes the quiescent current in the final stage through thermal feedback.

Figure 12 - VBE multiplier block.



The topology chosen, Figure 12, differs from the single-transistor VBEM by employing Q17 to maintain a more constant current magnitude across the sensor transistor (Q16), achieved by fixing its V_{BE} voltage across R25. To ensure effectiveness, Q17 must remain isolated from temperature variations. The purpose of R27 is to reduce the thermal compensation sensitivity and requires experimental adjustment through stress tests under maximum dissipation and resting conditions.

The selection of the 2SC3852A as the sensor transistor was motivated by its high h_{FE} current gain value of approximately 500 at room temperature, comparable to small signal BJTs. Available in a TO-220 package, it facilitates easy mounting on the heat sink.

Given that h_{FE} varies with temperature, minimizing base current variation is crucial to reducing error. High current gain at this position ensures negligible base current. Capacitor C6 is strategically placed to bypass the VBEM, maintaining a low-impedance path for the AC signal even at high frequencies (Cordell, 2019).

Output stage

The output stage topology selected was the triple emitter follower (EF3), a configuration designed to function as a high-bandwidth, low-distortion voltage follower (Locanthi, 1967). This topology consists of three sections: pre-drivers, drivers, and power BJTs.

Figure 13 illustrates the pre-drivers stage to the left of the red line and the drivers stage to the right. The power BJTs are shown separately in Figure 14.

Figure 13 - Driver and pre-driver sections.

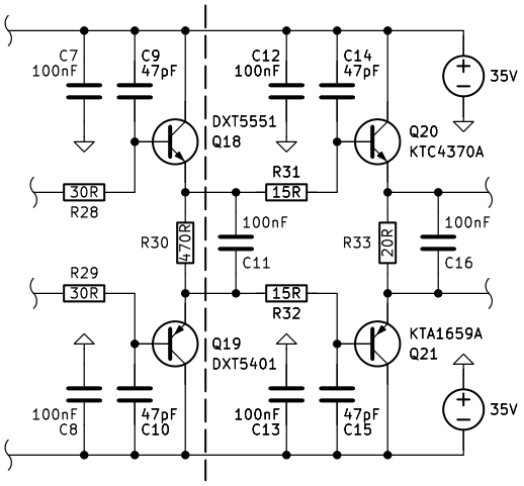
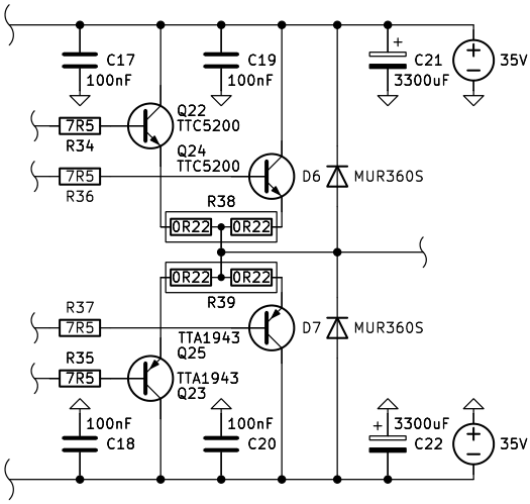


Figure 14 - Power BJTs section.

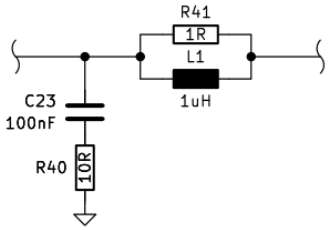


While a single pair of output transistors rated for 150 W would suffice for a 50 WRMS amplifier, two pairs were selected to enhance robustness and reduce large-signal non-linearities (Self, 2013). High-power BJTs, in particular, exhibit significant degradation in both h_{FE} and f_T as collector current increases. By paralleling multiple transistors and selecting parts that exhibit good gain linearity and high transition frequency, such as the TTC5200/TTA1943, the distortion introduced by the output stage can be effectively minimized.

The pre-drivers chosen were DXT5551/5401 for the same reasons that led to their choice as cascode transistors for the VAS, coupled with good gain linearity around the applied collector current. The drivers are KTC4370A and KTA1659A; these are medium-power, high-voltage parts ($V_{CE} = 180\,\text{V}$), packaged in an isolated TO-220 case, with current gain ($h_{FE} \approx 130$), capacitance ($C_{ob} \approx 25\,\text{pF}$) and transition frequency ($f_T \approx 130\,\text{MHz}$) suitable for the chosen operating point.

The resistors in the base-stopper function (R28, R29, R31, R32, R34, R35, R36, R37) together with the inclusion of base-collector capacitances (C9, C10, C14, and C15), shown in Figures 14 and 15, are intended to prevent the occurrence of local oscillations at the output stage.

Figure 15 - Arrangement of output filters.



The impedance presented to the signal source by a single emitter follower stage is given by equation (5):

$$Z_{IN} = (h_{FE} + 1) \times (r'_e + Z_L), \tag{5}$$

where Z_L is the load connected to the emitter, and the parallel associations $R_{30}||C_{11}$ and $R_{33}||C_{16}$ are the loads in question. Eventually, at a certain frequency, this RC load is transformed into a series combination between a capacitor and a negative resistance (Chessman & Sokal, 1976).

The inclusion of any inductive element forms an LC tank that will have its oscillation frequency infinitely amplified by the negative resistance part. To avoid this oscillation, an amount of resistance greater than $|Z_{IN}|$ must be added to the base of the emitter follower. Capacitors C9, C10, C14, and C15 were required to eliminate local oscillation, and their values were determined experimentally.

The current through the drivers and pre-drivers was chosen based on the relationship between collector current, transition frequency, gain linearity, and power dissipation. I_C was also chosen to keep these internships always working in Class A.

For the pre-drivers, $I_C = 5\,\mathrm{mA}$ was chosen because it provides good h_{FE} linearity and an estimated minimum of $f_T = 150\,\mathrm{MHz}$; these same reasons led to the choice of $I_C = 60\,\mathrm{mA}$ for the drivers, but for an estimated value of $f_T = 120\,\mathrm{MHz}$.

The current through the output devices was chosen to be around 120 mA and biases the BJTs in class AB, the emitter resistors assumed the ordinary value of 0.22 Ω, and non-inductive resistors (KOA SPEER BPR55 series) were used in this position.

Diodes D6 and D7 are a safety measure for directing high-voltage inductive pulses to the supply rails via a path around the power transistors. These diodes must withstand a reverse voltage greater than twice the rail-to-rail voltage and a current of at least 3 A (Self, 2013).

EMC output filters

At the output branch after the point where the feedback is taken, there are two filters, one being of the RC series type and the other of the RL parallel type, as shown in Figure 15. The R+C branch ensures stability in cases where the load becomes mostly inductive while the $R||L$ section compensates for situations where the load is excessively capacitive.

These situations are presented precisely by the load that the amplifier is intended to drive at all times; the speakers. The electrical model of a real load takes into account not only the electromechanical aspects of the speakers but also the geometry of the boxes in which the transducers are located, and results in an RLC model filled with reactances (Bortoni & Silva, 2003).

The values chosen were 10 Ω + 100 nF for the RC branch and 1 Ω || 1 μH for RL, these values are suitable for a wide range of conditions (Self, 2013). Both resistors are rated at 5 W and the inductor was wound with 12 turns of 12 AWG copper wire, resulting in estimated values of inductance $L = 1\,\mu H$ and resistance $R_{DC} = 3\,\mathrm{m\Omega}$ for a diameter of 15 mm and a length of 25 mm.

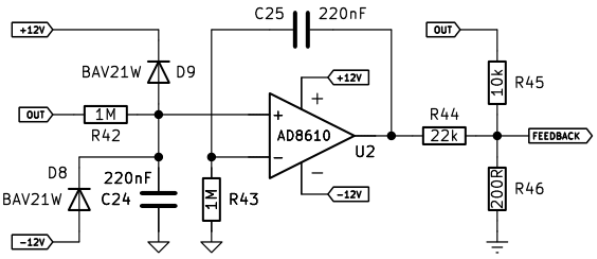
DC offset servo

It is common to find a capacitor in series with the resistor connected to ground in the feedback network. Its purpose is to act as an open circuit at DC so that the input voltage offset of the amplifier is not amplified by the gain set by the feedback network. The problem is that this capacitor needs to act as a low impedance at frequencies greater than DC and as the resistor in series with this capacitor tends to have a low value, this capacitor needs to have a very high value so as not to compromise the response at low frequencies.

This makes it impossible to use low distortion components such as film capacitors and class I dielectrics. As a result, this capacitor has been removed completely in favour of an active circuit that continuously corrects the offset at the output of the amplifier.

The servo circuit shown in Figure 16 is a non-inverter integrator with a very high time constant in order to ignore AC signals coming from the amplifier output, exclusively sensing the DC error. This error is then continuously integrated over time and applied to the inverting input of the power amplifier via an injection resistor (R44) that controls the servo feedback rate.

Figure 16 - Offset servo and feedback network.



The RC filter components are the same value pairs R42/C24 and R43/C25 that generate a cutoff frequency according to equation (6):

$$f_{C_L} = \frac{1}{2\pi R_{42} C_{24}} = 0.72\,[\text{Hz}]. \tag{6}$$

The value of R42 together with the supply voltage of $\pm 12\,\text{V}$ makes the servo capable of correcting offsets up to $\pm 110\,\text{mV}$ at the inverter input.

Diodes D8 and D9 direct possible high voltages in the direction of $\pm 12\,\text{V}$ rails to protect the input to the integrator and are general-purpose fast diodes for small signals. The operational amplifier used was the AD8610, as it does not exhibit phase inversion and has low noise, low voltage/current offset and extremely low input bias current (typically $I_{BIAS} = 3\,\text{pA}$).

The feedback network was designed, and the gain obtained by equation (7):

$$A_V = 1 + \frac{R_{45}}{R_{46}} = 51\,[\text{V/V}], \tag{7}$$

is equivalent to 34.15 dB. The value of the resistances was chosen as small as possible to minimize the contribution of Johnson-Nyquist noise on the system's amplification, but not low enough to generate excessive power dissipation.

Results and discussion

This section presents the detailed analysis of amplifier performance parameters, including thermal dissipation, frequency response, dynamic behavior, slew rate, harmonic and intermodulation distortions, and output noise. Initially, the maximum dissipation and junction temperature of the output components is calculated, followed by experimental verification of the frequency response and dynamic behavior for test signals. Next, the slew rate and the harmonic and intermodulation distortions are analyzed. Finally, the noise levels at the output and the behavior of the amplifier under clipping conditions and during the on/off transients are described, evidencing the high performance and stability of the circuit.

Dissipation

The worst case dissipation was calculated in SPICE for all the BJTs screwed to the heatsink and turned out to be a total of $P_D \approx 36\,\text{W}$. The estimated maximum junction temperature for the output devices is presented in equation (8):

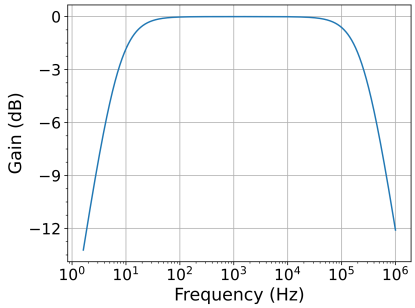
$$T_J = T_{AMB} + P_D \times (R_{\theta JC} + R_{\theta MICA} + R_{\theta HS}). \tag{8}$$

Taking $T_{AMB} = 50°\text{C}$ (ambient), $R_{\theta JC} = 0.83°\text{C/W}$ (junction-case), $R_{\theta MICA} = 0.1°\text{C/W}$ (mica insulator) and $R_{\theta HS} = 0.85°\text{C/W}$ (heatsink), we reach $T_J = 114°\text{C}$.

Frequency response

The response of the amplifier's closed-loop frequency was measured to check whether the input filter is the determining factor and whether the results match the values calculated in the "Input filters" subsection. Bode plot of the system's closed-loop response is shown in Figure 17.

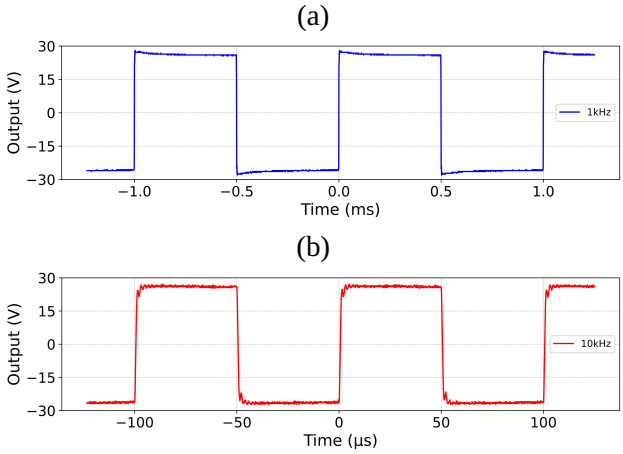
Figure 17 - Closed-loop frequency response.



Dynamic behaviour

The dynamic behaviour of two rectangular signals, one at 1 kHz and the other at 10 kHz, was also observed to identify potential instabilities. Figure 18 presents the shapes observed with the output at 50 W over an 8 Ω resistive load with the output at 50 W on an 8 Ω resistive load.

Figure 18 - Rectangular waves: (a) 1kHz (in blue), and (b) 10kHz (in red).

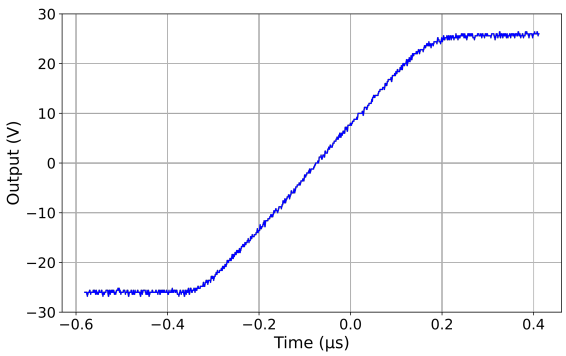


The behaviour of the 1 kHz wave, Figure 18(a), shows no overshoots or oscillations resultant from overshoots, while the 10 kHz wave, Figure 18(b), shows that there is no significant degradation to the speed of the edges or excessive rounding of the corners, indicating the adequate transient response of the amplifier.

Slew rate

Then, the SR was checked. Figure 19 presents the response of the rising edge to the maximum voltage excursion on an 8 Ω resistive load; the falling edge exhibited the same SR.

Figure 19 - Slew rate of the amplifier.



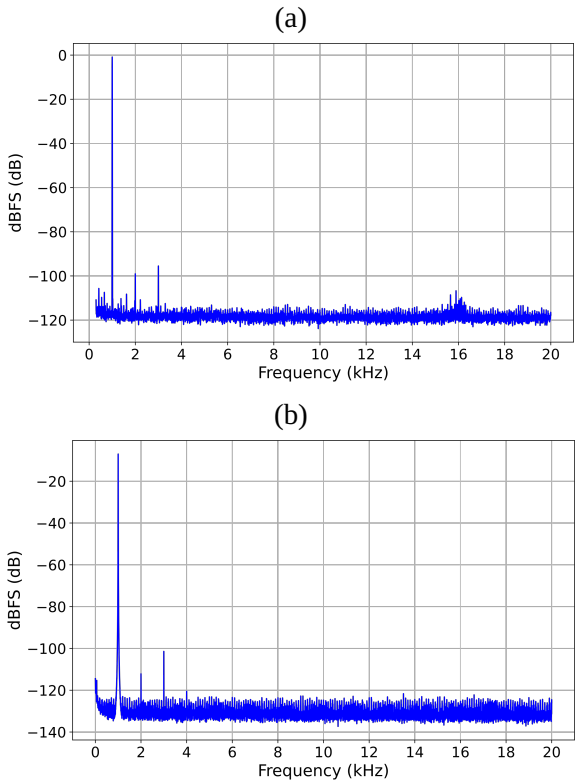
The measurement was carried out with the low-pass filter capacitor C2 removed so as not to impact the shape of the edges, resulting in a value of $107.4\,\mathrm{V}/\mu\mathrm{s}$, above the $39.6\,\mathrm{V}/\mu\mathrm{s}$ required for a $50\,\mathrm{W_{RMS}}$ amplifier to have a power bandwidth above $200\,\mathrm{kHz}$ (Duncan, 1996).

Harmonic distortion

Total harmonic distortion (THD) measurements were taken at 1 kHz for $P = 1\,W_{RMS}$ and $P = 50\,W_{RMS}$ using a USB capture card model Sound Blaster X-Fi HD (SB1240) manufactured by Creative Technology Ltd. and using ARTA software for data acquisition and processing (Artalabs, 2019).

Figure 20 present the frequency spectrum for output powers of 1 W and 50 W respectively, on the $8\,\Omega$ resistive load. The magnitude of the values is expressed in dB relative to the full scale (dBFS) of $1\,\mathrm{V}_{RMS}$ (0 dB) applied to the input of the acquisition board.

Figure 20 - Frequency spectrum: (a) 1kHz / 1W and (b) 1kHz / 50W



There is no visible difference in the absolute THD values obtained between the two tests, as seen by the height of the second and third harmonics, Figures 20(a) and 20(b). According to the measurements made by the ARTA software, the measured THD was only 0.0008%.

Intermodulation distortion

To measure intermodulation distortion (IMD), a complex signal consisting of two sinusoids of the same amplitude and frequencies of 10 kHz and 11 kHz was applied to the input of the amplifier, generating a modulated output of amplitude $V_O = 10\,\mathrm{V_{RMS}}$ on the $8\,\Omega$ resistive load, the result of which can be seen in Figure 21.

Output noise

Noise measurements were taken at the output of the system. The values obtained by short-circuiting the amplifier input were $15.2\,\mathrm{mV_{PP}}$ and $2.36\,\mathrm{mV_{RMS}}$. A summary of all measured parameters is shown in Table 1.

Figure 21 - Intermodulation spectrum $-10 + 11$ kHz.

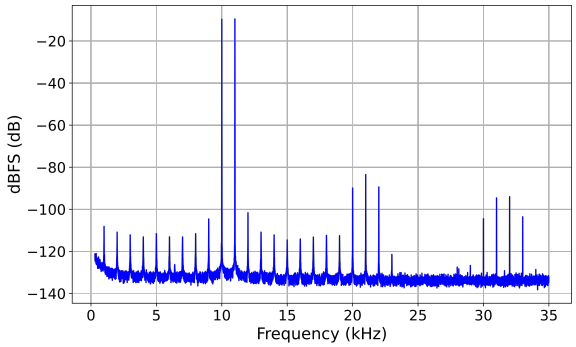


Table 1 - Measured parameters

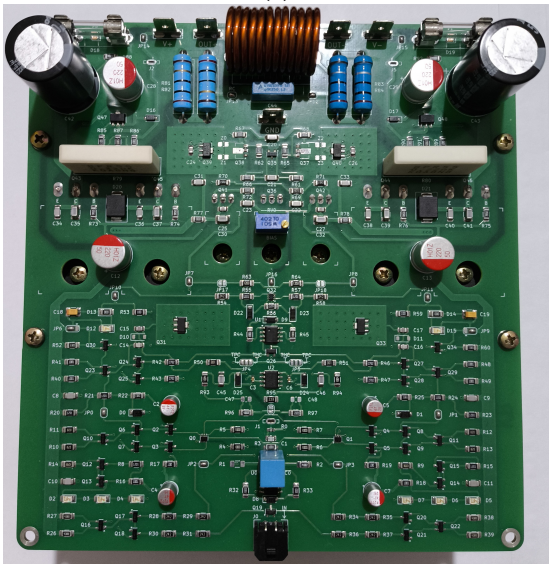
Description	Parameter	Result
Lower cutoff frequency	f_{CL}	7 Hz
Upper cutoff frequency	f_{CH}	255 kHz
Output noise (RMS)	$\text{noise}_{\text{RMS}}$	2.36 mV
Output noise (P-P)	noise_{PP}	15.2 mV
Slew Rate	SR	107.4 V/μs
Total harmonic distortion (THD) at 1 kHz / 1 W	$\text{THD}_{1\text{kHz}/1\text{W}}$	0.0015%
Total harmonic distortion (THD) at 1 kHz / 50 W	$\text{THD}_{1\text{kHz}/50\text{W}}$	0.0008%
Intermodulation distortion (IMD) at 10+11 kHz	$\text{IMD}_{10+11\text{kHz}}$	0.0065%

It was also noted that the amplifier exhibits smooth clipping behaviour, even when a sine wave severely overloads the input stage. The amplifier does not have a "thump" sound or exhibits oscillations during on/off transients, which are dangerous events for the speakers and especially for the tweeters. The offset servo also manifests no instability during the events.

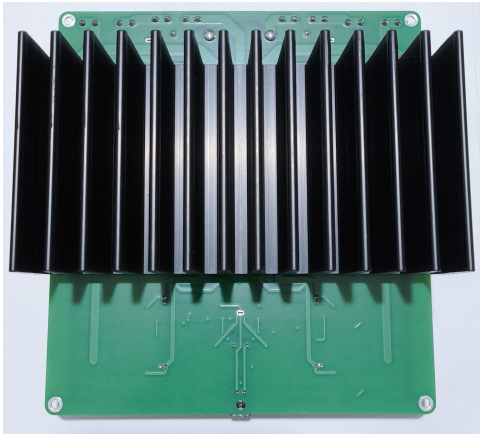
Figure 22(a) displays the component side of the built prototype, while Figure 22(b) shows the opposite side.

Figure 22 - Photo of the prototype: (a) top view, and (b) bottom view

(a)

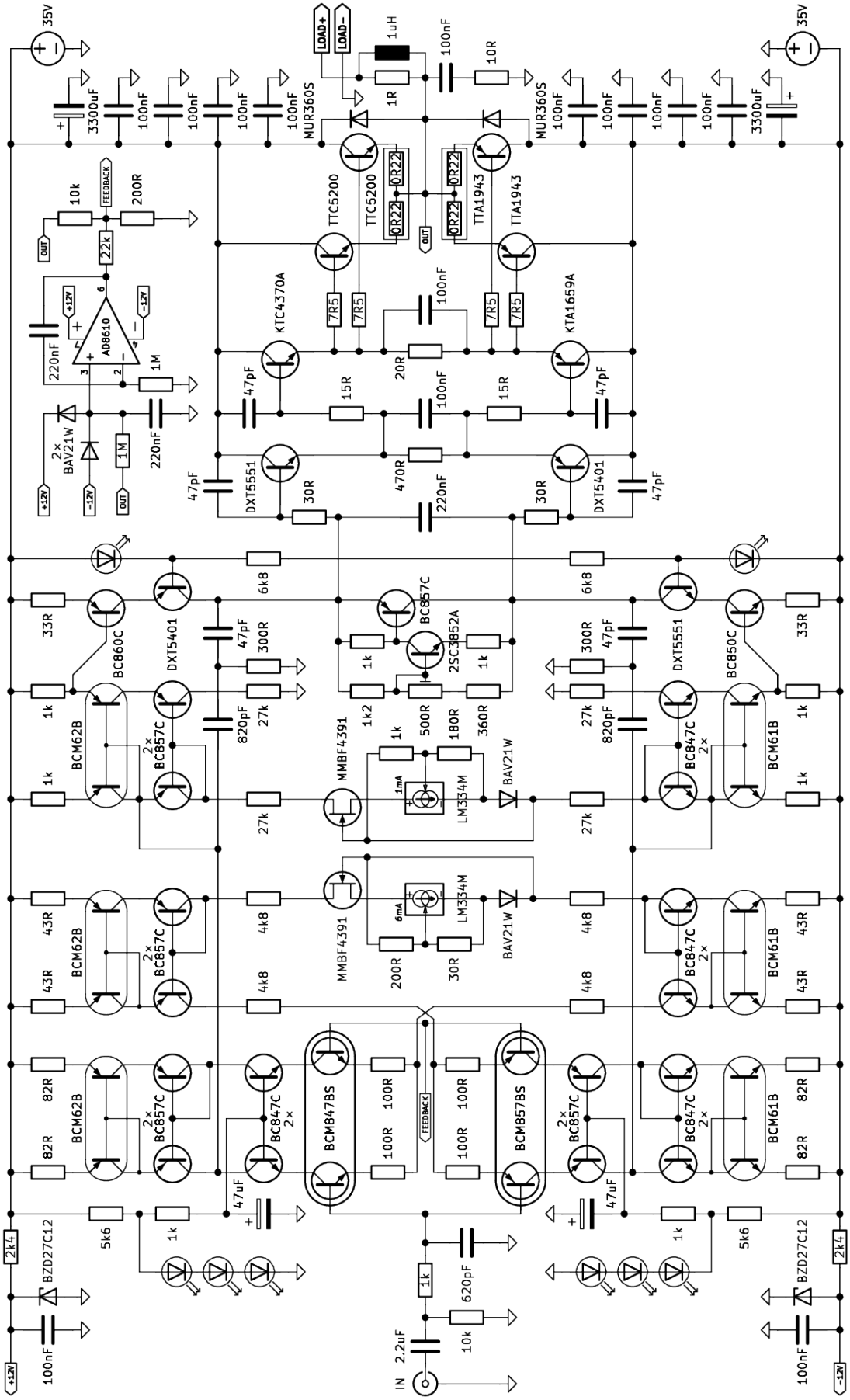


(b)



The complete schematic of the proposed topology is shown in Figure 23.

Figure 23 - Complete amplifier circuit.



Conclusion

The article has presented an innovative topology that enabled the use of active loads in the first differential stage by connecting it to a VAS-type gain stage without the use of gain limiting resistors. An amplifier circuit based on the presented topology was designed and assembled to validate this proposal, culminating in a functional prototype. The measurements performed confirmed the efficiency of the proposed topology, strengthening its practical viability. It is important to note that the prototype was built using the usual commercial components and the matching of semiconductor pairs was not carried out, making the topology a suitable choice for commercial applications.

It is also noteworthy that the scientific field related to the design and construction of audio power amplifiers is extensive, and many aspects have been omitted for brevity purposes.

Crucial elements such as power supply design, the board layout, and wiring planning are just as critical to achieving a high-level audiophile performance and deserve close attention in the implementation of high-performance projects.

Author contributions

A. S. Levorato contributed to: original idea, development, prototype assembly, editing and writing – original draft. **C. A. de Francisco** contributed to: methodology, supervision, writing – revision and editing.

Conflicts of interest

The authors declare that they have no known competing financial interests or personal relationships that could have influenced the work reported in this paper.

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