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A design methodology for audio amplifiers with no global negative feedback: Proposal and validation

Uma metodologia de projeto para amplificadores de áudio sem realimentação negativa global: Proposta e validação

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Abstract

This paper proposes a structured methodology for the design of high-performance audio amplifiers without the use of global negative feedback. This type of amplifier is being suggested in order to minimize supposed deleterious effects on audio quality. The proposed methodology uses a minimum number of stages with local negative feedback operating in a high voltage range in order to minimize harmonic distortion without the need to use global feedback. As an example of applying the methodology, a 50W power amplifier is designed and built. In this design example, three stages are used with field effect transistors operating with a symmetrical voltage of $\pm$90V in the voltage gain stages and $\pm$45V in the output stage. The practical results obtained satisfied the design requirements, such as: Slew Rate above 3.6V/μs (14V/μs), Upper Cutoff Frequency above 40kHz (125kHz), *THD+N* below 0.5% (0.2%). Also, to ensure that the designed amplifier has a good linearity, the IMD intermodulation distortion was measured. The value of -62.5dB was obtained. In this way, the effectiveness of the proposed method for the design of audio amplifiers without global negative feedback was proven.

Keywords: Audio amplifiers; power amplifiers; global negative feedback.

Resumo

Este artigo propõe uma metodologia estruturada para o projeto de amplificadores de áudio de alto desempenho sem o uso de realimentação negativa global. Este tipo de amplificador está sendo sugerido a fim de minimizar supostos efeitos deletérios na qualidade de áudio. A metodologia proposta utiliza um número mínimo de estágios com realimentação negativa local operando numa faixa de tensão elevada a fim de minimizar a distorção harmônica sem a necessidade do uso da realimentação global. Como exemplo da aplicação da metodologia, um amplificador de potência de 50W é projetado e construído. Nesse exemplo de projeto, são utilizados três estágios com transistores de efeito de campo operando com tensão simétrica de $\pm$90V nos estágios de ganho de tensão e $\pm$45V no estágio de saída. Os resultados práticos obtidos satisfizeram os requisitos de projeto, como, por exemplo: Slew Rate acima de 3,6V/μs (14V/μs), frequência de corte superior acima de 40kHz (125kHz), *THD+N* abaixo de 0,5% (0,2%). Ainda, para garantir que o amplificador projetado apresenta uma boa linearidade, foi medida a distorção de intermodulação IMD. O valor de $-62,5$dB foi obtido. Desta forma, foi comprovada a eficácia do método proposto para o projeto de amplificadores de áudio sem realimentação negativa global.

Palavras-chave: Amplificadores de áudio; amplificadores de potência; realimentação negativa global.

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Introduction

Since the beginning of audio amplifiers development, Global Negative Feedback (*G-NFB*), has been used with several advantages as: to control the amount of harmonic distortion, improve the stability of voltage gain, decrease output impedance, increase frequency response (SELF, 2009). This has happened since the first circuits with tubes, through bipolar transistors and modern field effect transistors (SINCLAIR, 2008). Most operational amplifiers used in audio applications also use *G-NFB* (HUIJSING, 2001).

Recently, the use of *G-NFB* has been criticized by the audiophile community. Signal compression, decreased spatial field and less musicality have been some of the deleterious characteristics pointed out by critics (ANALOG-PLANET. . . , 2019; PASS, 2008). One of the arguments used by critics of global negative feedback is the generation of higher order harmonics. Due to the non-linearities of the electronic components, 2nd (single-ended) and 3rd order (differential pair or push-pull) harmonics are generated. When these harmonics are fed back into the non-linear electronic components, high 4^{th}, 5^{th}, 6^{th} and 7^{th} order harmonics are generated at the system output, which are more detectable and less appreciable (MOIR, 1981; PASS, 2008). Following these arguments, some manufacturers of high-fidelity equipment have developed amplifier designs without *G-NFB* (DARTZEEL, 2019) and even with adjustable global feedback ratio (CH PRECISION, 2022). Circuit topologies used in these projects are protected by commercial rights and are not made available to the public. In this context, this paper discusses the main design criteria that can be used in the development of audio amplifiers without *G-NFB*. To exemplify the proposed criteria, a 50W audio power amplifier is designed, and its performance is evaluated.

In the next section, the proposed design procedure is presented in detail. Then, the procedure is applied to the design of a 50W audio amplifier. The designed amplifier is built and measured. The results are successfully compared with those simulated. Conclusions are presented in the last section.

Material and method

Design procedure

The proposed design procedure consists on the steps described below:

Step 1: Keep the minimum number of stages

This criterion guarantees the simplicity of the circuit, decreasing the degree of total distortion to be imposed on the audio signal and reducing the need for *G-NFB*.

Step2: Choose commercial transistors with high voltage specifications and use the maximum allowable working voltage

Operation with high working voltages allows the audio signal to make a low excursion at the polarization point. This causes the transistor to behave within the small-signal approximation. In this way, distortion is kept at low levels.

Step 3: Choose a topology with controllable amount of local feedback at each stage

The amount of distortion added at each stage must be controlled so that it is possible to obtain low levels of total harmonic distortion without the use of *G-NFB*. To achieve this, topologies with local negative feedback must be chosen.

Step 4: Optimize the stages for adequate frequency response, slew rate distortion and voltage gain

The amount of feedback set at each stage will affect all performance parameters. In this way, an optimization study must be carried out so that the circuit satisfies all the design criteria.

In order to validate the proposed methodology, the design, assembly and tests of a complete audio amplifier are described in the following section.

Design example

The performance criteria utilized for the current project are presented in Table 1, and the rationale for choosing each design requirement is presented below.

Table 1 – Design parameters.

Requisite	Value
Maximum power at 8Ω load	50Wrms
Upper cut-off frequency	> 40kHz
Lower cut-off frequency	< 10Hz
Minimum slew rate	> 3.6V/μs
Total harmonic distortion	< 0.5%
Input sensitivity	1Vp

Source: The authors.

The total output power was chosen to be 50Wrms as it is a usual value in audio amplifiers for home entertainment use. To achieve a low phase deviation, the frequency response was chosen to be one octave less than the minimum audible frequency (20Hz) and one octave above the higher audible frequency (20kHz).

The minimum slew rate, S_R, necessary to avoid transient distortion (SINCLAIR, 2008), can be calculated by equation (1)

$$S_R = 2\pi V_P f_{max}\ [V/s], \tag{1}$$

where V_P is the peak output voltage and f_{max} is the maximum frequency considered.

The peak voltage V_P at the output can be calculated by

$$V_P = \sqrt{2P_oR_L}, \tag{2}$$

where P_o is the output power and R_L is the load resistance.

To achieve an output power of 50W at 8Ω, using equation (2), results V_P =28.28V. Substituting V_P and f_{max} =20kHz in equation (1), we get S_R =3.6V/μs.

As the input sensitivity considered is V_{in} =1Vp, then the overall gain should be $A_{vT} = V_o/V_{in}$ =28.28. The maximum *THD+N* value considered here (0.5%) is half of the 1% indicated by the European Broadcasting Union (1998).

Results

The following show the results obtained in each step of the design process:

Result - Step 1: Keep the minimum number of stages

A complete Mosfet topology with only three stages was chosen. Details of the topology are presented in step 3.

Result - Step 2: Choice of commercial field effect transistors and the use of the maximum allowable working voltage

The 2n7000 signal Mosfet was chosen for the first stage due to its reasonable price and good performance. For the second stage the Mosfet pair IRF640/IRF9640 was chosen due to their high operating voltage and well-known application in audio amplifiers (INTERNATINAL RECTIFIER, [2022]). The same reasons determined the use of the IRFP240/IRFP9240 pair in the last stage.

Based on the transistor specifications, a voltage of ±90VDC was chosen for the first two stages, and ±45VDC for the power stage.

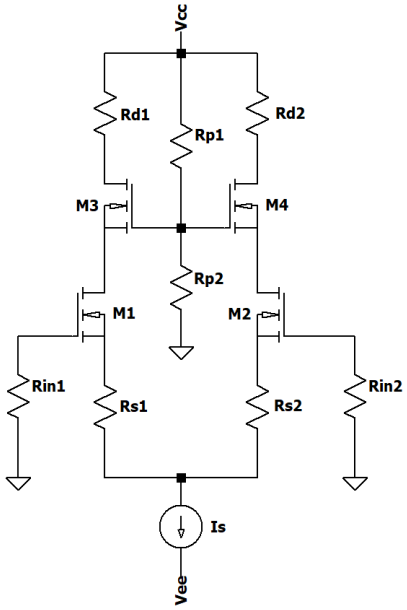
Result - Step 3: Choose a topology with controllable amount of local feedback at each stage

In the step 3, the three-stage topology is presented, being: Cascode differential amplifier, Cacode double amplifier and push pull buffer amplifier.

First stage: diferential Cascode amplifier

The first stage, shown in Figure 1, is a differential Cascode amplifier chose to handle a high bias voltage and provide a good frequency response avoiding the Miller effect.

Figure 1 – First stage topology: diferential Cascode amplifier.



Source: The authors.

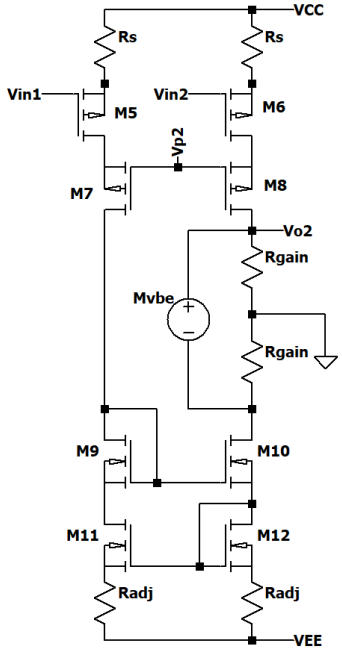
The bias voltage for Cascode transistors, M_3 and M_4, is chosen as $V_{cc}/2$ in order to minimize harmonic distortion by dividing the maximum excursion between the differential transistors, M_1 and M_2, and the Cascode pair.

Second stage: dual Cascode amplifier

The second stage, depicted in Figure 2, consists of two Cascode amplifier operating in counterphase by means of a current mirror also of the Cascode type, M_9 to M_12. As for the first stage, the bias voltage for Cascode transistors, M_5 and M_6, is chosen as $V_{p2} = Vcc/2$.

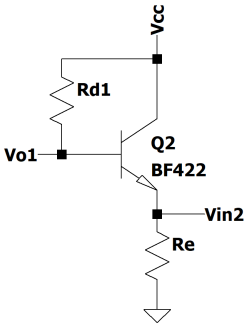
The first and second stages were buffered by a common collector transistor as shown in Figure 3.

Figure 2 – Second stage topology: dual Cascode amplifier.



Source: The authors.

Figure 3 – Bipolar common collector to buffer the first stage output.



Source: The authors.

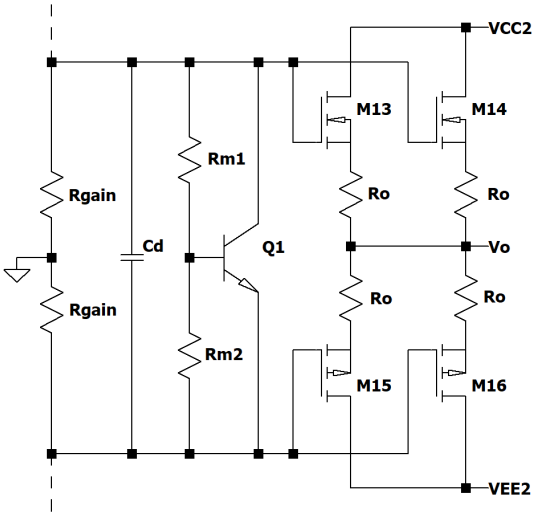
Third Stage: push pull buffer amplifier

The last stage is a regular push-pull current buffer. Third stage bias and thermal stability is provided by a V_{be} multiplier composed by Q_1, R_{m1} and R_{m2} as shown in Figure 4.

Result - Step 4: Optimize the stages for adequate frequency response, slew rate, distortion and voltage gains

A Python language program was developed to collect performance graphs through parametric variation (VAN ROSSUM, 2020). This program controls the LTSpice circuit simulation software which returns the desired performance parameters: distortion, slew rate and frequency response.

Figure 4 – Third stage schematic: push pull buffer amplifier.



Source: The authors.

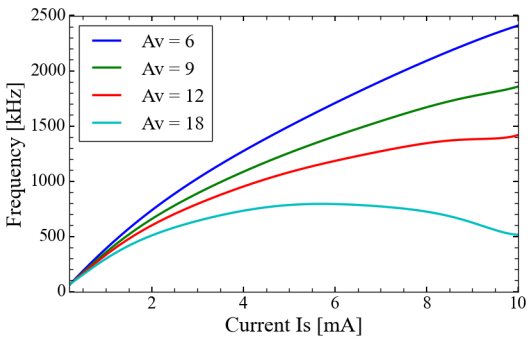
Circuit optimization was first performed at each stage separately. With these near-optimal values, the performance evaluation and optimization of the complete amplifier circuit was then carried out.

Circuit optimization - First stage: differential Cascode

The optimization process for the first stage was carried out by taking the current I_s[mA] and the voltage gain $A_v = V_o/V_{in}$ as variation parameters. The *DC* voltage across the Drain resistors R_d is fixed on 20V. This voltage will be used to polarize the second stage and was defined after some simulations as a good compromise between the gains in first stage and the amount of negative feedback to be obtained in the second stage.

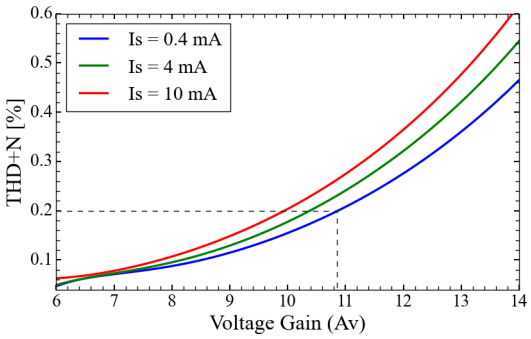
The upper cutoff frequency F_h[Hz], total harmonic distortion plus noise $THD+N$[%] and slew rate S_R[V/μs] were then obtained and the results are shown in Figures 5, 6 and 7.

Figure 5 – Cutoff frequency F_h as function of the quiescent current I_s for some values of the voltage gain A_v.



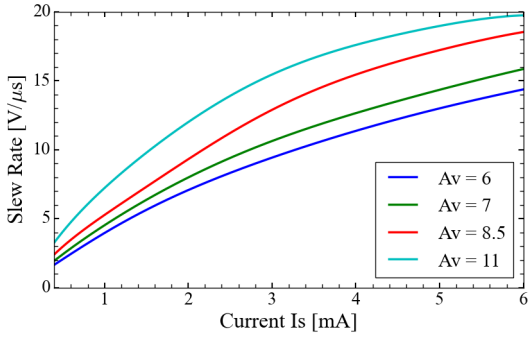
Source: The authors.

Figure 6 – Total harmonic distortion plus noise (*THD+N*) as function of A_v for some values of I_s.



Source: The authors.

Figure 7 – Slew Rate (S_R) versus source current (I_s) for some values of A_v.



Source: The authors.

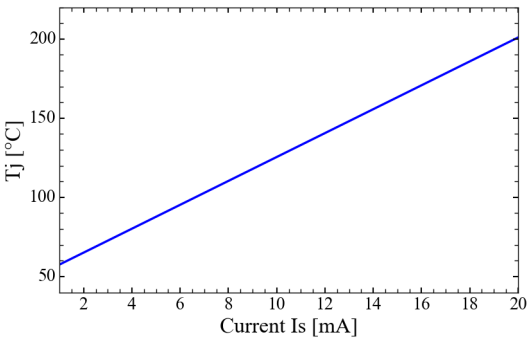
Figure 5 shows the upper cutoff frequency F_h[Hz] versus current I_s[mA] for various values of A_v. It can be noted the inversely proportional relationship between the voltage gain A_v and the cutoff frequency F_h. On the other hand, F_h increases for higher values of I_s. For the amplifier in question, a frequency response well above the audible upper limit is desired. This procedure also guarantees that the parasitic capacitances present in the practical assembly do not compromise the value of the cut-off frequency requested by the design requirements. So, a value of 100kHz was adopted. Analyzing Figure 5, it is possible to determine 0.4mA as minimum value for I_s.

Figure 6 shows the relationship between total harmonic distortion and voltage gain for some values of $I_s \geq$ 0.4mA. It can be seen that the *THD+N* increases with gain and current. It is safe to adopt a value of *THD+N* smaller than that required to ensure that practical effects not considered in the SPICE model do not deteriorate the results to the point of invalidating them. Thus, the value of 0.2% was adopted as maximum admissible distortion. Analyzing Figure 6, we see that the maximum voltage gain is limited to A_v =10.9 for a minimum current limit of 0.4mA.

Figure 7 shows the relationship between the slew rate S_R and the I_s and A_v parameters. It can be seen that low values of Is result in a low slew rate. High slew rate values, around 17V/μs, can be obtained for I_s values above 4mA.

As the power dissipation of the first stage transistors is proportional to I_s, the lower values are preferable because they cause a smaller temperature variation in the transistors. To study this influence, Figure 8 shows the relationship of current Is with transistor junction temperature T_j. If it is assumed a maximum of 80 °C to junction temperature, safely below the maximum 150 °C, the values of A_v =10.9 and I_s =4mA may be chosen as the quasi-optimal case.

Figure 8 – Estimated transistor junction temperature T_j versus current I_s.



Source: The authors.

After the optimization of the first stage, the same procedure was carried out for the second stage. The results are presented in the next section.

Circuit optimization - Second stage: Cascode voltage gain

The same design procedure performed for the first stage is repeated here for the second stage. In simulations, the resistor R_s, shown in Figure 2, is used to define the drain current and the voltage gain is controlled by the resistor Rgain. The voltage source Mvbe represents the V_{be} multiplier circuit to be used to polarize the third stage.

The same optimization procedure was repeated for the second stage, where the stages were optimized for adequate frequency response, slew rate, distortion and voltage gains. The only difference is that the voltage gain of the second stage is determined by the overall gain of the amplifier. The total gain of the amplifier is given by

equation (3)

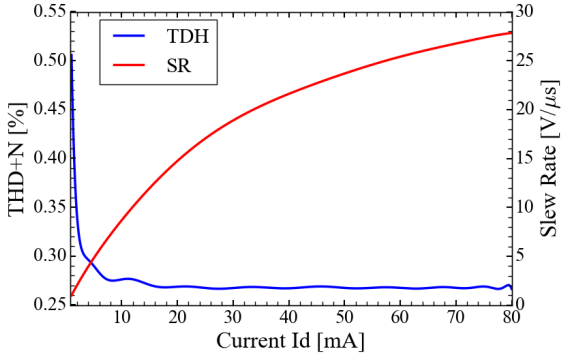
$$A_{vT} = A_{v1}A_{v2}A_{v3}, \quad (3)$$

where A_{v1}, A_{v2} and A_{v3} are the voltage gains for the first, second and third stages, respectively.

Considering $A_{v3} \cong 0.83$, typical value, and $A_{v1} = 10.5$, previously calculated, then $A_{v2} \cong 3.25$. This gain was then used in simulations which results are summarized below.

Total harmonic distortion and the slew rate, S_R, as function of the current I_d[mA] are plotted in Figure 9.

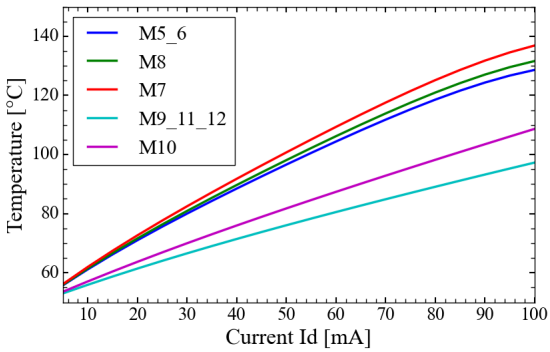
Figure 9 – Total harmonic distortion (blue line) and slew rate (red line) behavior as function of the second stage drain current I_d.



Source: The authors.

It may be noted that great values of I_d will result in greater S_R, which is desirable, but there is no significant improvement on *THD* for values of I_d above 20mA. On the other side, power dissipation may be a constraint. Figure 10 shows the dependence of the junction temperature on I_d for all the second stage transistors. In these calculations, the use of *HS7021* heatsink was considered (HS DISSIPADORES, 2022).

Figure 10 – Transistor junction temperature as function of the second stage drain current I_d for transistors M5 to M12.

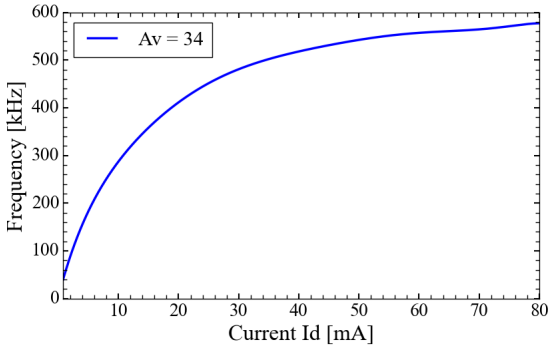


Source: The authors.

Using the same procedure as for the first stage, we can assume a safe junction temperature of 80 °C. In this case, the drain current is I_d =27.5mA. This value implies a S_R =18.1V/μs. Although the minimum S_R required is 2V/μ s, some authors indicate an allowance of 0.5V/μS per peak output volt (V_p) (DUNCAN, 1997). As shown earlier, the output voltage for 50W at 8 ohms is V_{op} =28.28V. In this case, the indicated slew rate would be $S_R = 0.5V_{op}$ =14.14V/μs, justifying the choice for I_d.

The third parameter to be analyzed is the upper cutoff frequency F_h. Figure 11 shows F_h dependence on I_d.

Figure 11 – Upper cutoff frequency as function of the second stage Drain current I_d.



Source: The authors.

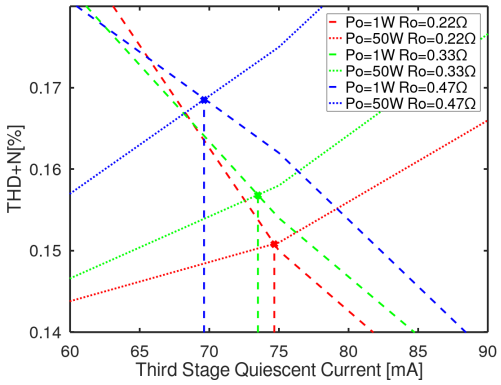
It can be seen in Figure 11 that for I_d =27.5mA is expected F_h =467kHz, well above the minimum required (F_h > 40kHz). It is worth mentioning that the cut-off frequency predicted in the simulation does not include the parasitic capacitances that are dependent on the practical assembly. Therefore, in practice, a lower cut-off frequency is expected.

Circuit optimization - Third stage: class AB buffer

To optimize the third stage, the value of the output stage resistor R_o and the bias current I_{DQ} must be chosen in order to minimize distortion and slew rate. At low power operation, crossover distortion dominates, while high-excursion distortion dominates at high powers.

To find the optimal value for R_o and I_{DQ}, the total distortion at 1W (low power) and 50W (high power) were calculated for some values of R_o as a function of I_{DQ}, shown in the Figure 12.

Figure 12 – Distortion as a function of polarization current I_{DQ} for P_o =1W and 50W for three values of R_o.



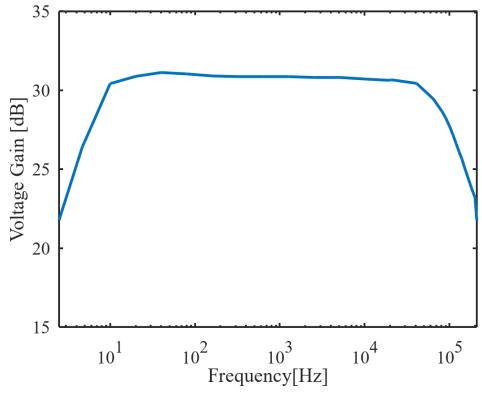
Source: The authors.

The crossing points, in the Figure 12, indicate the current that implies same distortion at low and high powers. Also, it can be observed that lower values of R_o result in lower values of distortion, however, to ensure good thermal stability, the value of R_o =0.33Ω was adopted. In this condition, the value I_{DQ} =73.8mA results in a uniform distortion as a function of the output power. It is worth mentioning that other design criteria can be adopted, such as minimizing distortion at low power. This can be accomplished by using smaller bias currents at the expense of greater distortion at higher power levels.

Measurements

The final circuit was implemented in a circuit board and the performance parameters were measured. The amplifier frequency response, shown in Figure 13, was measured at 50W output power. The measured low and high cutoff frequencies were F_L =6Hz and F_h =125kHz, respectively.

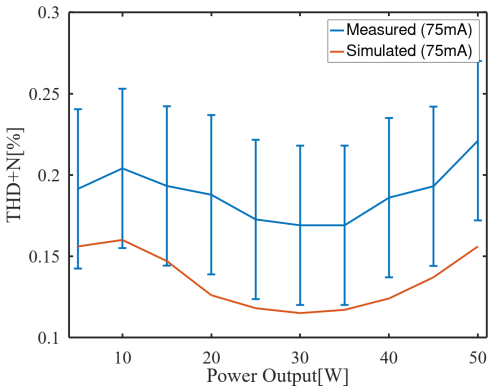
Figure 13 – Measured amplifier frequency response.



Source: The authors.

The measured and simulated values of *THD+N* as a function of output power, for a standard 1kHz sinusoidal signal, are plotted in Figure 14.

Figure 14 – Measured and simulated Total Harmonic Distortion plus Noise *(THD+N)* for output power values from 1 to 50W.

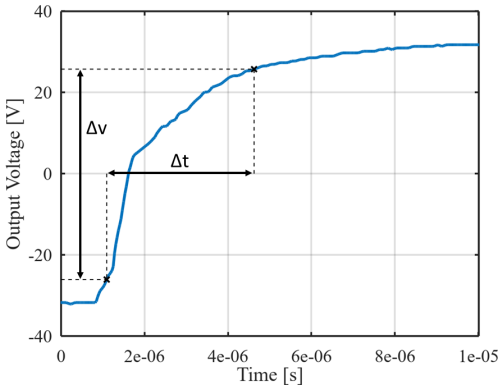


Source: The authors.

It can be seen Figure 14 that the measured values follow the same pattern as the simulated ones. The small difference between the curves is mainly due to the intense electromagnetic noise present in the laboratory that is not taken into account in the simulations.

There are several ways to measure slew tate on audio amplifiers. In this work, a worst-case methodology is used. A rectangular signal with 2V peak-to-peak and f =1kHz is inserted into the amplifier and the temporal response analyzed, as shown in Figure 15. The slew rate is then calculated by measuring the voltage variation between 10% and 90% of the total excursion Δv[V] and dividing by the time variation Δt[s].

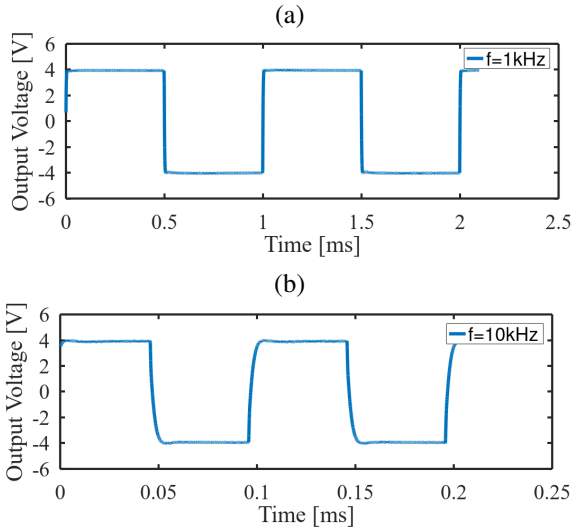
Figure 15 – Measured temporal response at full output excursion, $V_{in} = 2V_{pp}$.



Source: The authors.

In the example shown in Figure 15, the voltage variation measured is Δv =51.84V and the time variation Δt =3.53μs, resultingin S_R =14.68V/μs. To exemplify the temporal behavior of the amplifier, Figure 16(a)-(b) shows the output voltage for rectangular input signals with amplitude of 8Vpp and frequencies of 1kHz and 10kHz. It can be verified that there are no rings or oscillations of any kind and, for 10kHz, the signal is fast enough, with little deformation.

Figure 16 – Amplifier output square waves at: (a) 1kHz and (b) 10kHz, $V_o = 8V_{pp}$.



Source: The authors.

Despite not being one of the specified design requirements, the Intermodulation Distortion (IMD) was measured in order to ensure that the designed amplifier have good linearity without the use of global negative feedback. To measure the IMD, it was used the Twin-Tone IMD technique resulting in the CCIR parameter (HONGWEI, 2020).

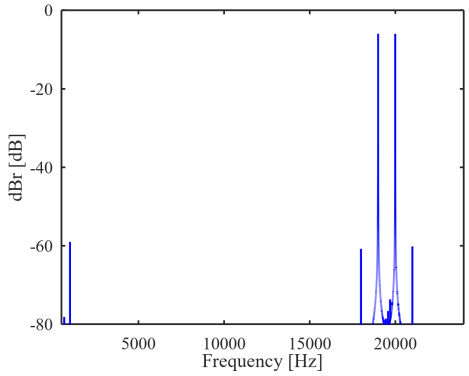
Two sinusoidal signals of 19kHz and 20kHz were introduced into the amplifier in order to output 25W each. Beat frequencies were then measured. Figure 17 shows the amplitude spectrum in the output.

The intermodulation parameter calculated was CCIR = − 62.5dB. This result ensures good linearity with no global feedback. It is worth noting that the amplifier can still be optimized to reach some other performance criterion through the already generated graphics.

However, as summarized in Table 2, the amplifier met all the design requirements, demonstrating the effectiveness of the proposed methodology.

The complete amplifier scheme is depicted in Figure 18.

Figure 17 – Amplifier Intermodulation Spectrum, 19kHz+20kHz at 50W into 8ohms.



Source: The authors.

Table 2 – Comparison of measured and simulated parameters.

Parameter	Requisite	Simulated	Measured
F_h [Hz]	> 40k	257k	125k
S_R [V/μs]	> 1.2	17.4	14.7
THD+N [%]	< 0.5	0.152	0.22

Source: The authors.

Conclusion

Because the amplifiers do not have negative global feedback, it is advisable to use servo amplifiers to ensure a low offset voltage. Other precautions that also apply to the usual amplifiers must also be adopted, such as the use of gate resistors in the Mosfets to avoid self-oscillation and a proper adjustment of the thermal compensation of the last stage to avoid thermal runaway.

The methodology proposed in this work is intended to serve as a basis for designers to carry out amplifier designs without global negative feedback including topologies with tube devices or bipolar junction transistors. Other design requirements can be added to the proposed steps targeting a specific application without affecting the methodology itself. In conclusion, we hope to have contributed to the area of analog circuit development, as the design methodology proposed in this work provides a basis for designers to develop amplifier circuits without the use of global negative feedback.

Acknowledgments

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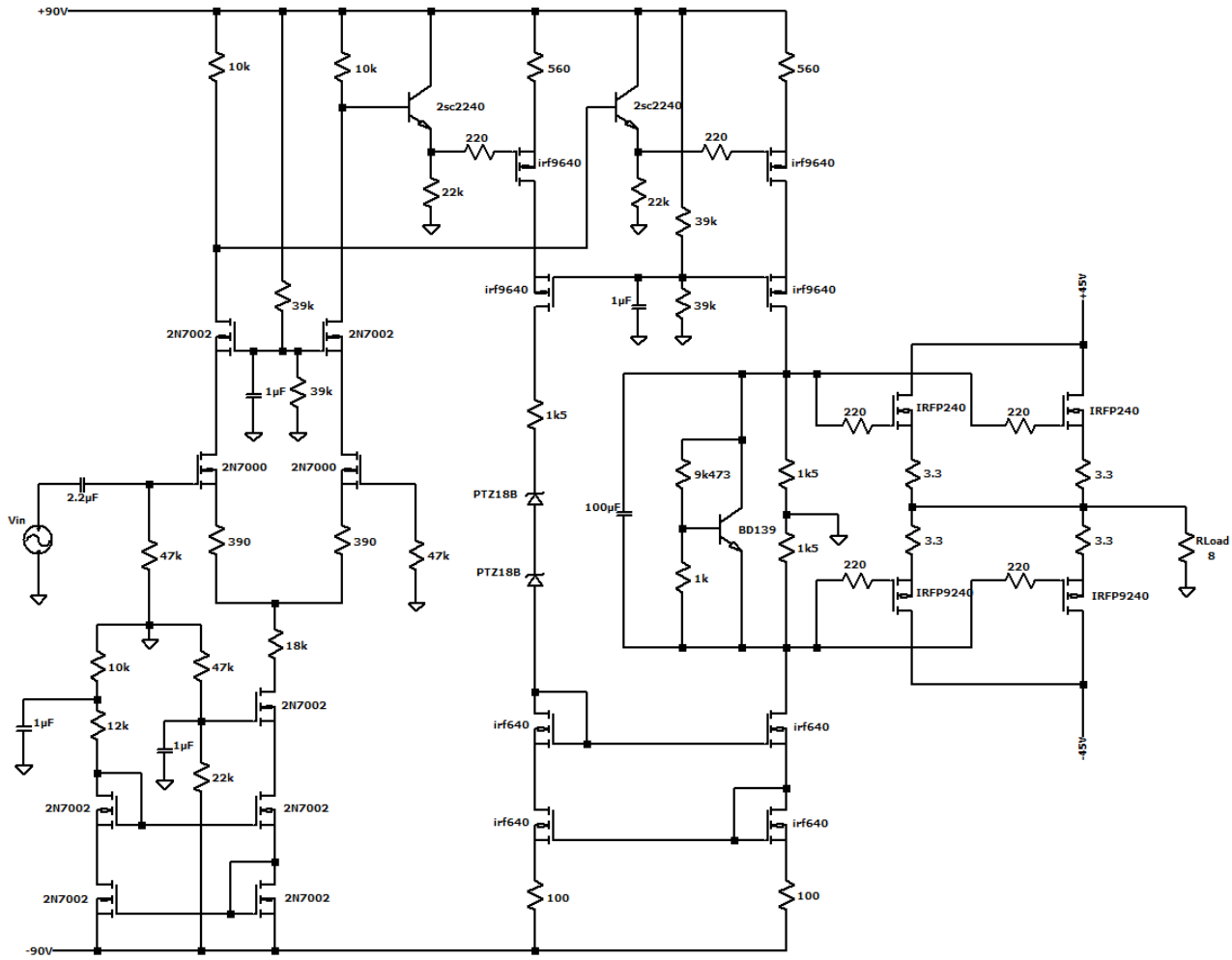
Figure 18 – Complete audio amplifier scheme.



Source: The authors.

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