Ambiente de programação descrito em VHDL para célula de memória analógica do tipo Floating-Gate

VHDL-based programming environment for Floating-Gate analog memory cell

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Resumo

Um ambiente de programação desenvolvido em VHDL para células de memória analógicas do tipo CMOS *Floating-Gates* é apresentado. Uma malha de controle digital compara o alvo pré-ajustado pelo usuário com o estado atual do *Floating-Gate* e através da aplicação de pulsos controlados, o novo valor analógico é memorizado. Este circuito pode ser utilizado em células de *trimming* analógico em aplicações VLSI, onde o pós-processamento do circuito integrado é proibitivo devido aos altos custos envolvidos.
Palavras-chave: Floating-Gate. Trimming. VHDL.

Abstract

An implementation in CMOS technology of a Floating-Gate Analog Memory Cell and Programming Environment is presented. A digital closed-loop control compares a reference value set by user and the memory output and after cycling, the memory output is updated and the new value stored. The circuit can be used as analog trimming for VLSI applications where mechanical trimming associated with post-processing chip is prohibitive due to high costs.
Key words: Floating-Gate. Trimming. VHDL.

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Introduction

Floating Gate Transistors (FGMOS), which appeared in 1967 as a non-volatile data storage element (KAHNG; SZE, 1967), have been mostly used in digital circuits as storage devices and in analog signal processing by exploiting the weighted-sum property of its multiple inputs (SHIBATA; OHMI, 1993). It also finds application in low-voltage circuits due the fact that its equivalent threshold voltage can be tailored to desired values and in neural networks systems (ANDREOU; YANG, 1994). The FGMOS is compatible with standard CMOS technologies. The appealing feature of this device in the point of view of analog signal processing is the possibility of modifying its current-voltage characteristic in non-volatile way by changing the amount of charge that is stored in the floating gate, performing as an analog memory cell (HASLER; BRADLEY, 1999).

Analog memories have some advantages over digital ones: smaller area, lower power consumption and higher dynamic range. As a disadvantage, to program an analog memory it requires longer time and a precise control to guarantee the writing of the correct value.

This paper describes an analog memory cell based on FGMOS, including the high-voltage transistors needed to program the FGMOS, implemented in a standard CMOS process.

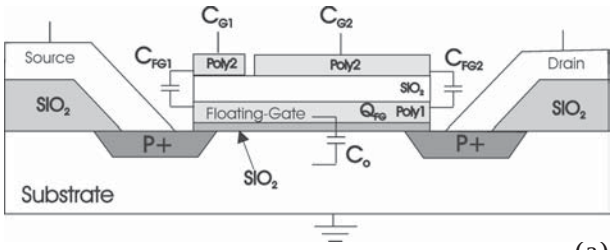
Floating Gate MOS Transistors

The basic structure of an FGMOS is a conventional MOS transistor with the gate completely involved by SiO2 (and is then called a floating gate). Capacitors coupled to the gate, as shown in Figure1(a), control the gate voltage by capacitive coupling. The other terminals of the coupling capacitors (C_{G1} and C_{G2}) are called control gates. Figure1(b) shows a floating-gate device built in 0.6μm technology. The effective gate-source voltage or the floating-gate voltage is given in (1). In this case, only two control gates are considered, but the generalization is still valid for *i* control gates.

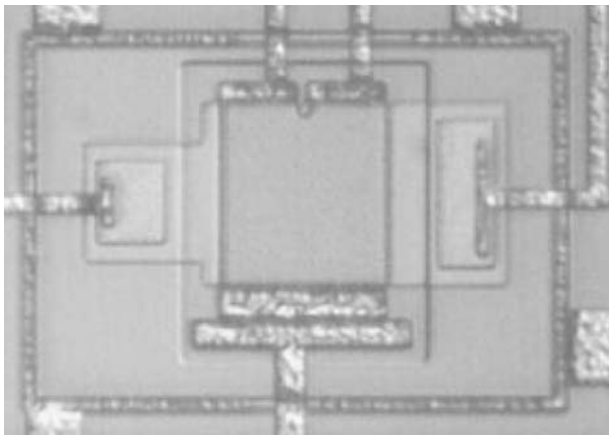
$$V_{GSEFF} = V_{FG} = \sum_i k_i.V_i + \frac{Q_{FG}}{C_{TOT}}$$

$$C_{TOT} = \sum_i C_i = C_{FG1} + C_{FG2} + C_O \qquad (1)$$

In (1), $k_i=C_i/C_{TOT}$, V_i and C_i are the voltage and the capacitance of the control gate *i* respectively, Q_{FG} is the charge trapped in the floating gate and C_{TOT} is the total capacitance of the gate.



(a)



(b)

Figure 1. Floating Gate (FGMOS) Device.
(a) Cross-section of a FGMOS transistor.
(b) Photomicrograph of a FGMOS device in 0.6mm technology.

These trapped charges are the element used to retain information in an FGMOS memory cell. These charges don't change for operating voltages inside the normal range of the technology (5 V for 0.6 μm). As indicated in (1), the transistor effective threshold voltage V_{TH} can be changed either by using one of

the control gates as V_{TH} controller or by changing the stored charge Q_{FG} in the floating gate by applying high voltage programming pulses to the floating gate capacitor (COUTO; CAJUEIRO; REIS, 2003). The second approach allows the implementation of non-volatile V_{TH}-based analog memories. Figure 1(a) shows schematically the first technique where an applied voltage to the control-gate (select gate voltage in the 0-5V range) controls the threshold voltage whereas Figure 1(b) shows experimental results from a FGMOS device built in 0.6μm technology to the changes in stored charge Q_{FG} (after application of high-voltage programming pulses in 12V-15V range). This device will be used in the implementation of the non-volatile V_{TH}-based analog memory cell as proposed in this work. In reading circuits, the effective threshold V_{TH} can be detected through either the variation on the gate voltage for a constant drain current or as a variation of the drain current for the same gate voltage.

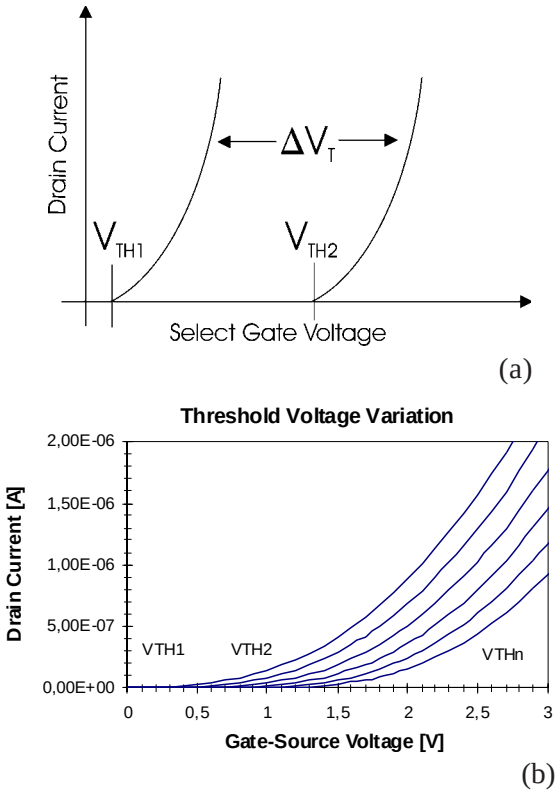


Figure 2: Variation of the effective threshold voltage. (a) Using one of the control gates. (b) Changing the trapped charge.

To write in this memory means to change the trapped charge. This is possible by applying a voltage pulse (setting an electric field) to the control gate high enough to tunnel electrons through the oxide. By using two control gates, it is possible to apply only positive pulses for programming the floating gate transistor as depicted in Figure 3. Applying high voltage pulses (V_{HIGH}) to the C_{G1} while grounding C_{G2}, the electric field is almost entirely applied across the smaller-area capacitor C_{FG1} and electrons may leave the floating-gate poly by tunneling across the dielectric. Therefore, Q_{FG} decreases and so does the threshold voltage. On the other way around, applying pulses on the C_{G2} while grounding $C_{G1,}$ the electric field polarity reverses and Q_{FG} increases and so does the threshold voltage (BRADLEY; MINCH; DIORIO, 2001).

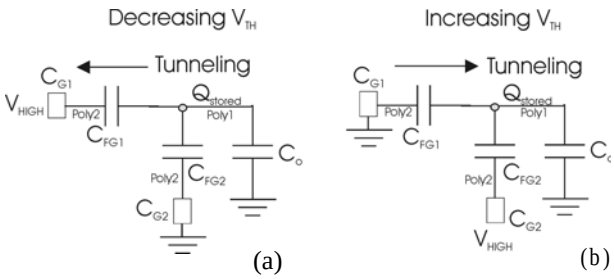


Figure 3. Programming the FGMOS using two controlling gates. (a) Decreasing V_{TH}. (b) Increasing V_{TH}.

The result of this programming technique is shown in Figure 4 for a device built in 0.6 μm technology. It is worth noting that there is an exponential behavior of the programming scheme, e.g., for the first pulses, there is a greater change in threshold voltage. As long as more charges are built up, the storing process becomes less effective for the same applied electric field. It is refereed in literature as self-limiting process (COUTO; CAJUEIRO; REIS, 2003).

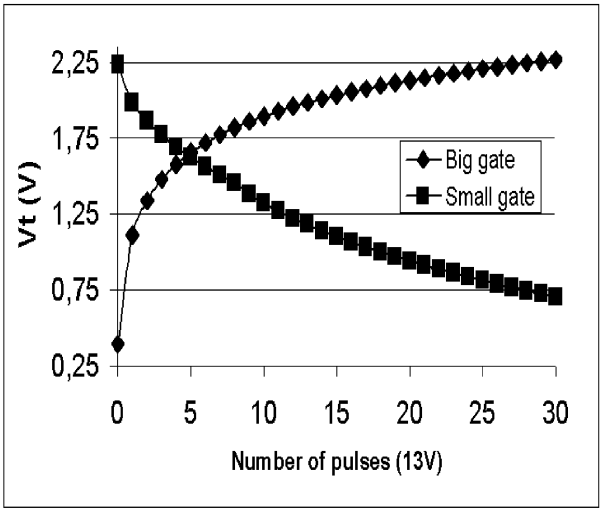


Figure 4. Change in V_{TH} for 1msec-13 V pulses applied to the control gates.

Analog Memory Core

The FGMOS transistor can be used to implement an analog memory cell based on the transistor threshold voltage reading. The threshold voltage can be modified according the programming pulses that either increases or decreases the electric charge Q_{FG} in the floating gate poly. Additionally, a reading circuit should be used to read either a current or voltage based on the aforementioned threshold voltage V_{TH}. Therefore, it is presented an analog memory cell based on FGMOS whose gates are sized to allow omni-directionality programming pulses (only positive voltages used). This cell also uses high-voltage transistors to withstand the high-voltage used for programming the FGMOS. The high voltage transistor is a LDD (light doped drain) MOS and can stand voltages up to 25 V for AMS 0.6 μm CUB process[3]. This core allows the implementation of a very compact memory cell for trimming purposes on a single chip.

The FGMOS implemented is based on poly1-nwell capacitor (available in standard CMOS process). In the used technology, the inter-poly oxide thickness is 40 nm - too thick for electron tunneling. Hence, for the employed 0.6 mm technology, the control gate capacitors were formed between poly1 and n-well, presenting an oxide thickness of 16 nm and thus requiring lower tunneling voltage (lower dielectric voltage barrier). The programming voltage is near 12-13 V, a suitable voltage range for the LDD MOS withstand.

The analog memory cell core is shown schematically in Figure 5(a). The circuit presents Read and Write modes of operation. In Read mode, M1 and M2 gates (C1 and C2) are high (5V); Both LDD MOS transistors are conducting and so does the FGMOS transistor. The resulting FGMOS current develops the output voltage over R_o. As mentioned before, the FGMOS current depends on the stored-charge-based threshold voltage. Therefore, the output voltage is the memorized analog value of the memory cell. On the other hand, in the write mode, the FGMOS threshold voltage can be changed and so does the output voltage for the next reading cycle. By grounding either control gates C1 or C2, the high voltage applied causes the electrons to tunnel into or out the floating-gate poly so changing the threshold voltage. After a period for stabilization, the circuit enters into read mode until new analog value is to be stored. Figure 5(b) shows the simulated output voltage of the memory cell in reading mode after programming in writing mode. To improve the resolution of the analog memory, short-programming pulses should be used. However, due to self-limiting programming process, a great number of pulses must be used in order to the memory reach the desired value in a very time-consuming mechanism. To get practical results, the programming process must be automatic, i.e., once the volatile target is set up, the memory seek the same value to be stored. Next section will address this automatic control.

[3] This is a proprietary technology from AustriaMicrosystems.

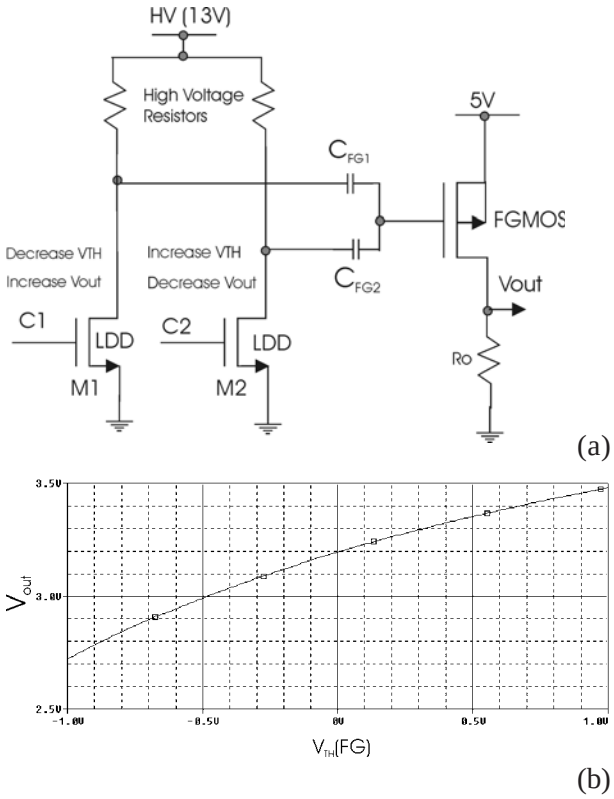


Figure 5. Analog Memory Cell. (a) Memory Core. (b) Memory output versus programmed threshold voltage.

Control Circuit

In order to make the programming process automatic, a controlling mechanism was implemented using a commercial FPGA (Field Programmable Gate Array) and an Analog-to-digital A/D converter (ADC0804) to adjust the memory output to any desired value within an allowable range. In this case, the analog value to be memorized corresponds to an 8-bit reference, which is set up only for programming purposes. Notwithstanding the fact that commercial devices were used, this non-volatile analog memory can be fully implemented in any standard CMOS regarding the programming process can be accomplished in different ways. The proposed system is depicted in Figure 6(a). The FGMOS memory output voltage is read by the A/D converter and compared to the reference value to be stored. The FPGA-implemented algorithm sets the controlling gates (C1 and C2) to adjust the cell output voltage to the chosen reference value. Once the target is reached, the digital reference can be removed. The control program inside the FPGA is quite simple as can be seen in fluxogram of Figure6(b).

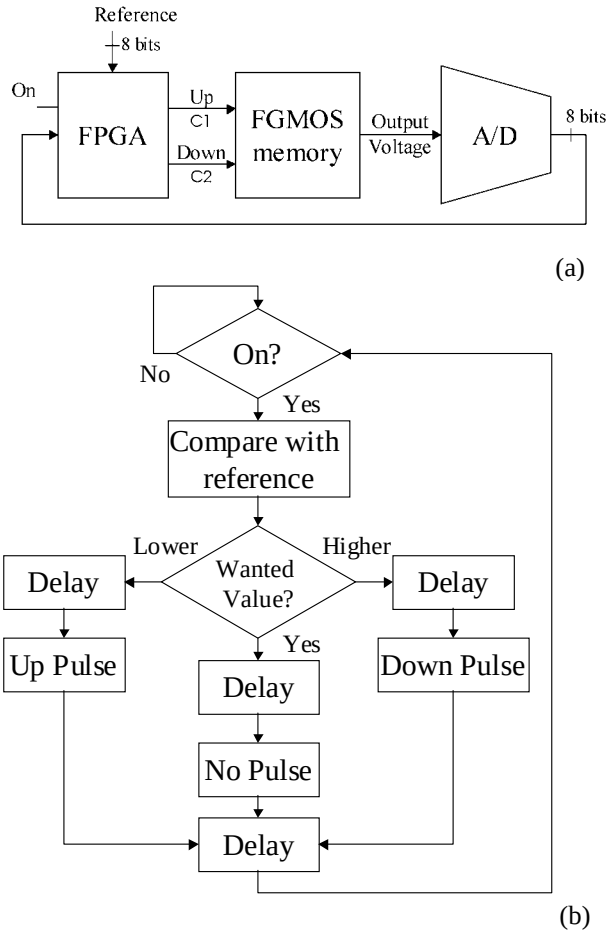


Figure 6. Analog Memory Cell Implementation: (a) FGMOS memory cell programming environment. (b) VHDL-based controlling algorithm.

The output voltage range varies from 2.5 to 4 V, thus the A/D is adjusted to have this same range (the ADC0804 allows it through the pins VIN- and VREF/2). Since it is an 8-bit converter, this means that its resolution is of 5.86 mV per bit, so we can adjust the output memory cell with a precision of less than 6 mV.

To circumvent the self-limiting effect, the algorithm seeks the target value indefinitely up to the 6mV resolution window. This makes the target-reaching time variable according the target value. A time out is set if, for any reasons, the analog output

fails to reach the required value. The pulse width chosen was 10 ms, an experimented value according the tradeoff between resolution and programming time. The variation of voltage obtained with this pulse width is always smaller than 1mV, thus preventing the system to oscillate. Time delays are needed because the output voltage is not valid while the cell is being programmed. Therefore, there must be a minimum time to the cell reach a valid value. All the delays were set to be 500ms, but they can be smaller. Figure 7 shows the timing diagram of the implemented algorithm using VHDL description for the FPGA circuit.

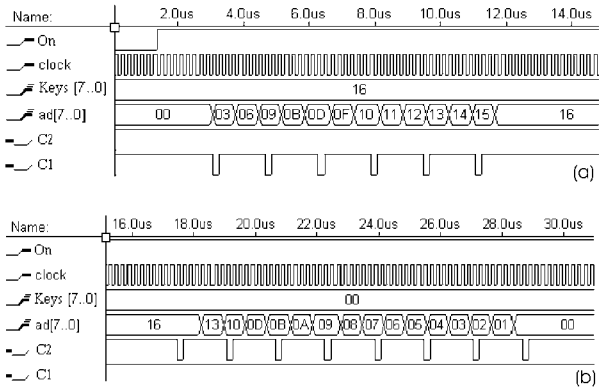
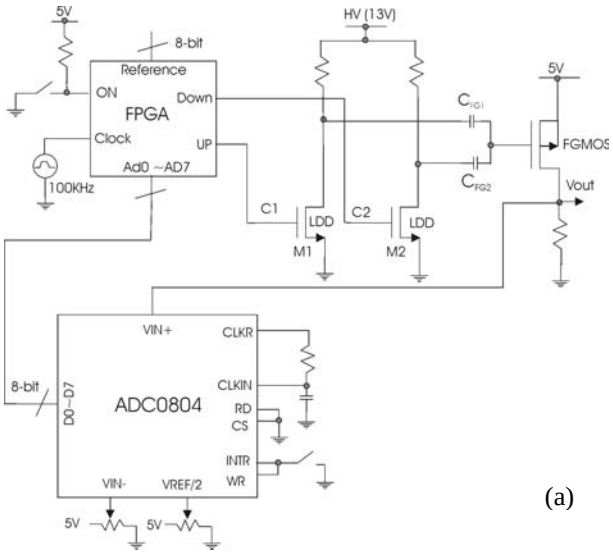
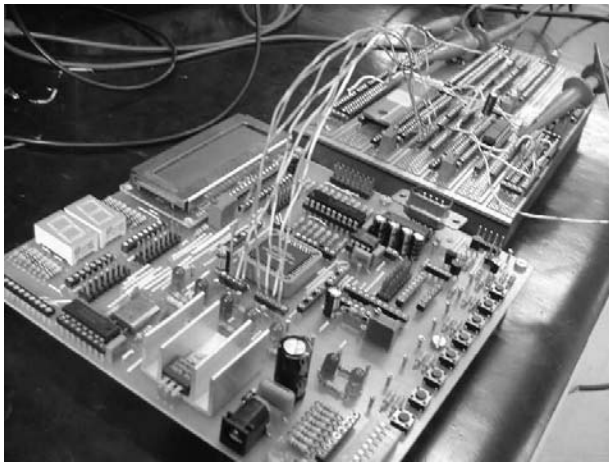


Figure 7. Timing diagram. (a) Increasing the memorized value. (b) Decreasing**.**

Starting at "On" signal on, a three level comparison (higher, lower and equal) is enabled between "Keys" and "ad" signals. The result sets a low level for either C1 or C2 gates, depending on the comparison result thus enabling the memory cell to be programmed. When the comparison results equal value for "Keys" and "ad" signals the system is halt and the programming process stops, moving to the reading mode. The new stored value is read on memory output.

The complete schematic circuit is presented in Figure 8(a). Excluding the A/D converter and the FPGA all other components were integrated into a chip implemented in AMS-CUB 0.6mm technology. The FPGA circuit used was the EPM7032SLC44-10. The fully circuit implementation showing the development board for FPGAs testing is shown in Figure8(b). This environment includes some facilities as LCD displays, keys, clock generators, etc.





(b)

Figure 8. Implemented Circuit. (a) Schematic. (b) Development and testing board.

Experimental Results

Aiming to validate the proposed implementation, the analog memory was programmed to follow several targets. The output voltage changed as expected. In all tests carried out the error between memorized value and reference sets was smaller than 10 mV. Figure 9(a) shows the variation of the output voltage responding to a decrease in the reference, while Figure 9(b) is the same for an increase in the

reference. The pulses width and delay were changed for better visualization in time domain. It is shown that during the writing time, the output analog memory is not valid.

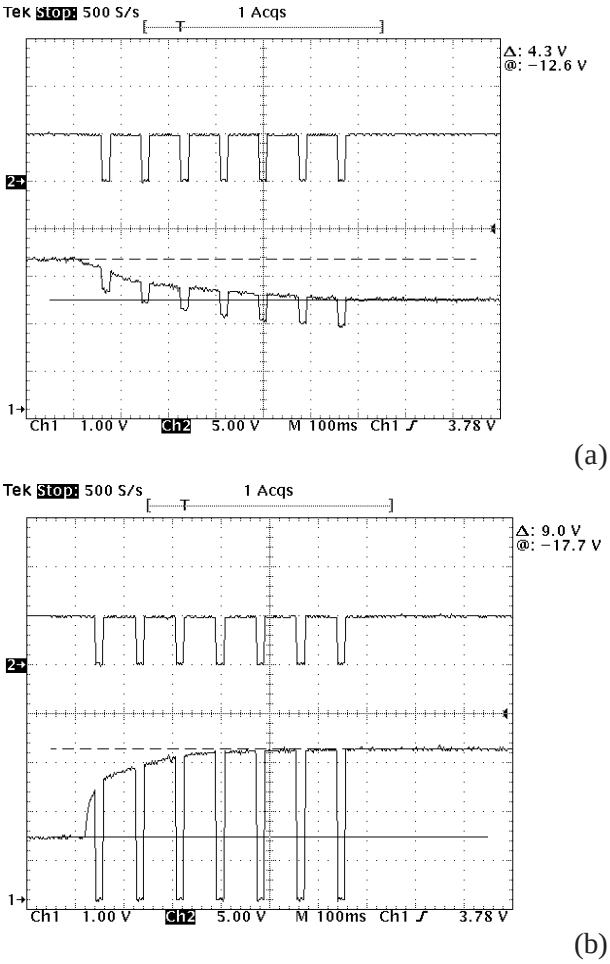


Figure 9. Analog Memory cell Results. (a) Decrease in the reference. (b) Increase in the reference**.**

Figure10 presents the photomicrography of the memory analog cell implemented in AMS-CUB 0.6μm technology. The cell includes the FGMOS, resistors and LDD transistors.

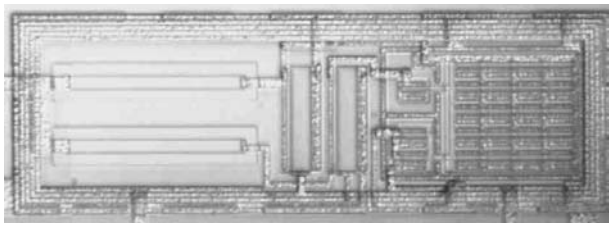


Figure 10. Photomicrography of the analog memory cell

Conclusions

An analog memory cell based on Floating-Gate transistors devised for trimming purposes is implemented and tested. A Field programmable gate array (FPGA) and an Analog-to-digital converter were used to complete the programming environment. The results suggest that fully integrated versions can be thought as practical implementations in mixed signal integrated circuits such as Smart-Power applications. The analog memory cell can outperform functions that otherwise digital approach would be very complex.

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